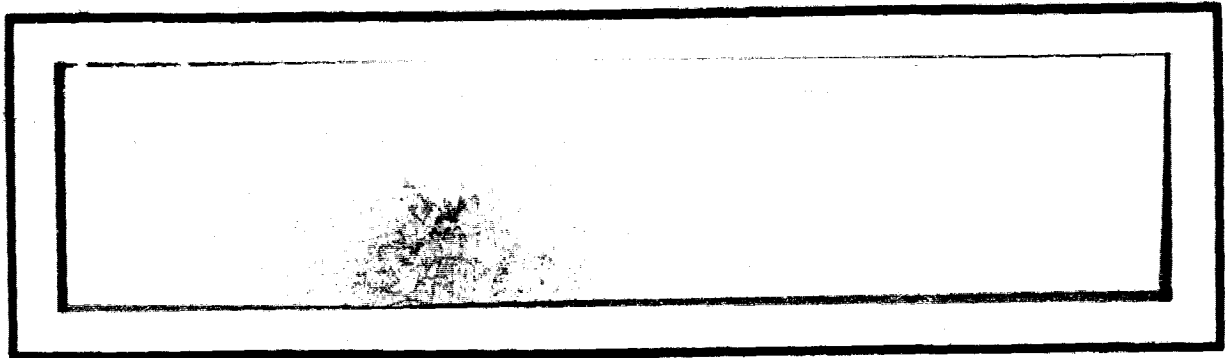


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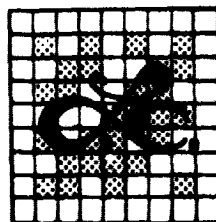


(NASA-CR-161009) ORBITER GLOBAL POSITIONING
SYSTEM DESIGN AND KU-BAND PROBLEMS
INVESTIGATION, EXHIBIT E, REVISION 1
Interim Report (LinCom Corp., Pasadena,
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ORBITER GLOBAL POSITIONING SYSTEM DESIGN
AND KU-BAND PROBLEM INVESTIGATIONS
EXHIBIT B - REVISION 1

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SUMMARY

This report serves to document the LinCom effort under Exhibit B of Contract NAS9-16097 in supporting the JSC study of the use of the GPS navigation system on the Space Shuttle and in Ku-band problem investigations. LinCom has been tasked to evaluate system implementation, performance, and integration aspects of the Shuttle GPS system and to provide independent technical assessment of reports submitted to JSC regarding integration studies, system studies and navigation analyses. The results of this effort is contained primarily in a set of five memos [1]-[5] and a report [6]. In addition, an ongoing effort is to review and evaluate the DoD Joint Program Office GPS Phase II User System Specification [7] and the Space Shuttle Orbiter/GPS Procurement Specification [8]. Documents [1] to [6] are attached for reference.

1.0 EFFORT RELATED TO GPS

In support of the Ku-band program, LinCom was tasked to evaluate the effect of coaxial cables and connections on the data waveform, to perform an analytical investigation of bit synchronizer and phase-offset correction circuitry, and to investigate discrepancies between predicted and measured performance parameters as test data becomes available.

1.1 Conference Support

LinCom participated as a representative of JSC in the GPS Constellation Conference at SAMSO on June 5, 1980. The purpose of the GPS Constellation Conference was to address the budget-driven program change to reduce the number of satellites from 24 to 18 in the GPS network. Its impact on the Space Shuttle program in terms of Shuttle mission schedules and Shuttle navigation via GPS were documented in [1].

We did not attend the Magnavox Phase II PDR due to attendance space

limitations. However, we have reviewed the PDR notes (taken by Dr. Jim Pawlowski and Howard de Vezin) and provided preliminary comments [3]. Since the two-channel set is functionally similar to the Shuttle GPS R/PA baseline, some effort was spent on interpreting and understanding the TTFF procedure for the two-channel set and the results were documented.

1.2 GPS General Support

Support was provided to JSC on analytical and/or technical questions regarding GPS development implementation and performance. These efforts are highlighted as follows.

The timing structure of the received GPS signal was summarized to highlight its impact on the normal acquisition procedure and time-to-first-fix (TTFF). In particular, the handover procedure from C/A-code to P-code was addressed. The results were documented in [2].

The problems and options associated with testing the GPS receiver were investigated in [5]. In particular, the emphasis was on testing the GPS receiver when only one simulated emitter signal (out of a total of a complete set of four) is available. The ideal test configuration and the basic system and subsystem tests required to determine receiver performance were described. The implications of testing with a nonideal configuration, for example, with 1 satellite simulator, were then considered. Special attention was devoted to the 2-channel sequential set (present JSC baseline). Supplementary tests that can be performed independent of the simulator signals were also highlighted.

A simple sequential one channel set was recommended for JSC breadboard development. The rationale was documented in [3].

In [4], a hardware and software method for obtaining bit and

subframe synchronization were proposed. The hardware method was recommended for the GPS breadboard development program.

1.3 Analytical GPS Modelling

In order to support the hardware development and implementation of the bit and frame synchronizer [4], we have analytically modeled these synchronizers. The results from this analysis are provided in [6] and should be useful in setting system parameters pertinent to their acquisition behavior and detection performance.

1.4 Recommendations for Additional Areas of Investigative Effort

LinCom should continue to identify and study key system parameters relating to the performance of the Shuttle/GSP R/PA such as: (a) Time-to-first-fix (TTFF), (b) acquisition strategies and (c) various tracking loop parameter for PN tracking, carrier tracking, bit synchronization and frame synchronization. One major purpose of the analytical study is to parallel and support the review and critique of the R/PA procurement specifications as they evolve. LinCom should also continue to follow the GPS JPO Phase II efforts in order to keep track of current developments and identify techniques, hardware problems and areas of concern which are of interest to the Shuttle GPS program.

Two additional areas were uncovered during this phase of our efforts and they deserve further investigation. One area is the study of the R/PA system performance testing requirements and procedures. In particular, an understanding of the required test equipments, e.g. GPS signal simulators and R/PA test access points are needed. Another area is concerned with the hardware design support for the ESTL GPS receiver development program undertaken internally at JSC.

2.0 EFFORT RELATED TO KU-BAND SYSTEM

2.1 Ku-Band Analytical Simulation

LinCom has developed an analytical simulation of the RG-142 coax cable which supports data transmission on the 2-to-50 Mbps channel. The analytical simulation accounts for cable attenuation, input asymmetry, data/clock offset, input amplitude variations, rise and fall times, and transition density. The simulation was developed in such a manner that the cable pulse output features can be assessed and used in the development of a specification to be supplied to the Ku-band vendor. A time error budget was established in support of the new design of the mid-bit data reclocking circuitry. The results of this simulation are documented in Section 3 of this report. In addition, LinCom supported numerous Ku-band technical reviews at Hughes Aircraft and Rockwell International, as required by JSC.

2.2 Ku-Band Analytical Investigations

LinCom has performed an analytical investigation of the bit synchronizer and phase-offset correction circuitry presently recommended by the Ku-band vendor. Particular attention was given to the false-lock problem to which the current design is susceptible. The cable output distortions and their impact on the performance of the Ku-band mid-bit/phase correction circuitry were evaluated. The results of this study are documented in Section 4 of this report.

2.3 Ku-Band Test Data Evaluation

LinCom has performed investigations of discrepancies between theoretical performance predictions and measured values. To this end, LinCom analyzed the available test results, performed analytical performance predictions and reported on the major discrepancies and

their possible origins.

A major effort was undertaken in the analysis of autotrack test data. The findings were reported to NASA/JSC [10-12] and Rockwell International [9].

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3.0 RG142B CABLE RESPONSE TO 50 MBPS DATA STREAM IN THE PRESENCE OF COAXIAL CONNECTORS

Introduction

An analytical computer simulation model for the transfer function of a coax cable was developed in a previous LinCom memo⁽¹⁾. The objective of this report is to extend the previous model to a case where coaxial connectors are present. The analytical model of a connector for bit rates under consideration is developed using the manufacturer supplied voltage standing wave ratio associated with the connector. The connector and the cable models are employed in a software package to study and predict the signal distortions caused by the line. It is shown that presence of a few connectors (<10) will contribute very little to the amplitude loss or other distortions introduced by the line.

1. Analytical Model for RG142B Coaxial Transmission Line in Presence of Coaxial Connectors

For data bit rate of 2-50 Mbps, a coaxial cable can be modeled as a linear system with transfer function $C(\omega)$:

$$C(\omega) = e^{-\gamma l} \quad (1)$$

where γ is a constant depending on the cable and l is the cable length. It is shown that if (1) is utilized for RG142B cable, the amplitude loss at 50 MHz equals 2.7 dB⁽¹⁾. To consider the connector role, one

can take advantage of the specifications chart provided by the connector manufacturer. At the bit rate under consideration, the most useful information provided for a connector is the voltage standing wave ratio (VSWR) because using this ratio the reflection coefficient can be computed. From the tests performed by different manufacturers, it is apparent that the VSWR of coaxial connectors is linear in frequency, and, for the sake of simplicity, one sample is selected to be used in this report. According to SOCAPEX⁽²⁾ catalog a SMA connector for RG142B/U cable demonstrates the following VSWR:

$$\text{VSWR} = 1.1 + .02F \quad (2)$$

where F is the frequency in GHz. The relationship between VSWR and the reflection coefficient ρ is given by

$$|\rho| = \frac{\text{VSWR}-1}{\text{VSWR}+1} \quad (3)$$

To derive the transfer function equation associated with a connector with reflection coefficient ρ , we observe that the reflected wave contains a reflected power term P_n given by⁽³⁾

$$P_n = |\rho|^2 P_+ \quad (4)$$

where P_+ is the input power. Transmitted power P (power passing through the connector) can be computed as

$$P = P_+ - P_n = (1-|\rho|^2)P_+ \quad (5)$$

Since the power is proportional to the square of the voltage⁽⁴⁾, thus the following equation can be deduced from (5)

$$V^2 = (1 - |\rho|^2) V_+^2$$

where V is the transmitted waveform voltage and V_+ is the input voltage. The ratio V/V_+ defines the connector transfer function $H(\omega)$,

$$H(\omega) = \frac{V}{V_+} = \sqrt{1 - |\rho|^2} \quad (6)$$

Equation (6) is the model for a coaxial connector. The above model does not take into account the R.F. leakage or any other losses since the frequency of interest is rather low (considerably less than 1 GHz).

Because of the linearity of the overall system, a cable of length L plus n connectors demonstrate the following total transfer function

$$H_T(\omega) = C(\omega) H^n(\omega) = e^{-\gamma L} (1 - |\rho|^2)^{n/2} \quad (7)$$

where $|\rho|$ is given by

$$|\rho| = \frac{.1 + .02F(\text{GHz})}{2.1 + .02F(\text{GHz})} \quad (8)$$

Equation (7) is used in a simulation program to predict the system response to different input patterns. Figure 1 displays the magnitude of $H_T(\omega)$ for two different conditions; plot a is obtained assuming no connectors on the line, while plot b assumes 9 connectors are present. At 50 MHz, the amplitude loss increase because of 9 connectors is approximately .1 dB.

2. Total System Response

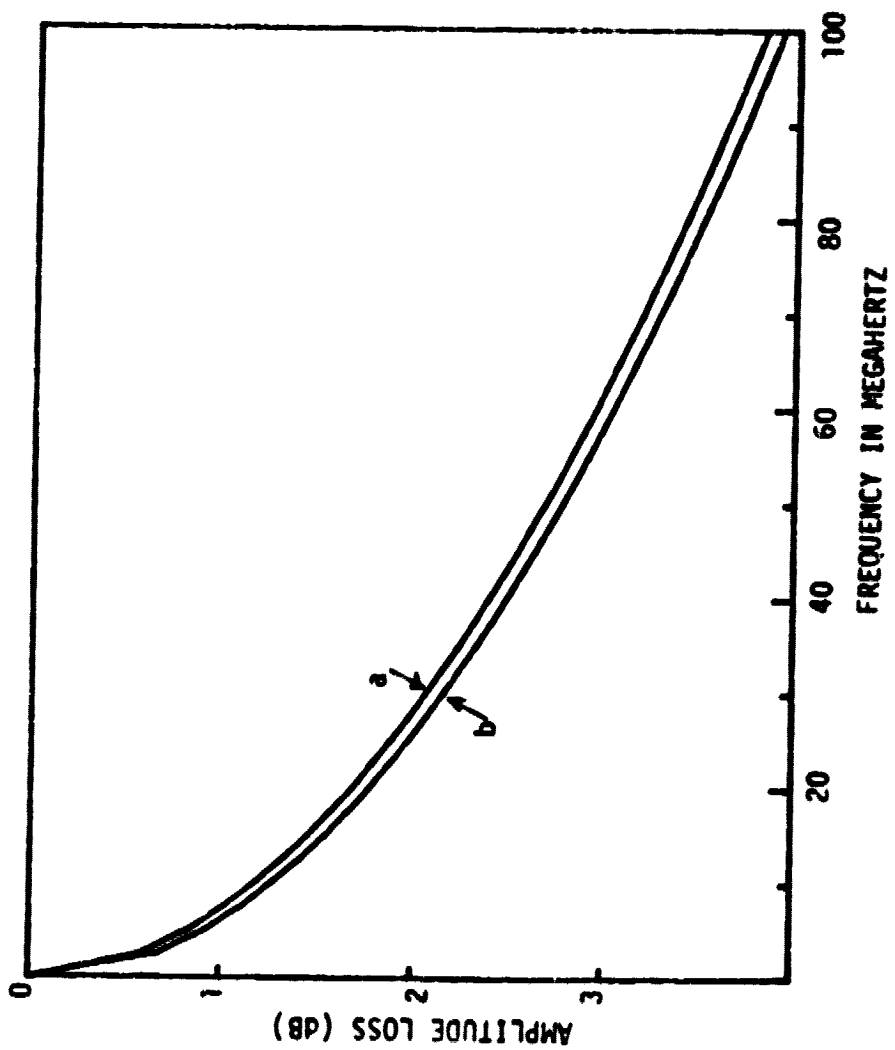
Figure 2 shows the system response to a trapezoidal shape pulse of width 20 ns and 3 ns rise time. The three plots correspond to no connectors on the line, 9 connectors on the line, and 99 connectors on

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Figure 1.

a: Connectors are not used

b: 9 connectors are used



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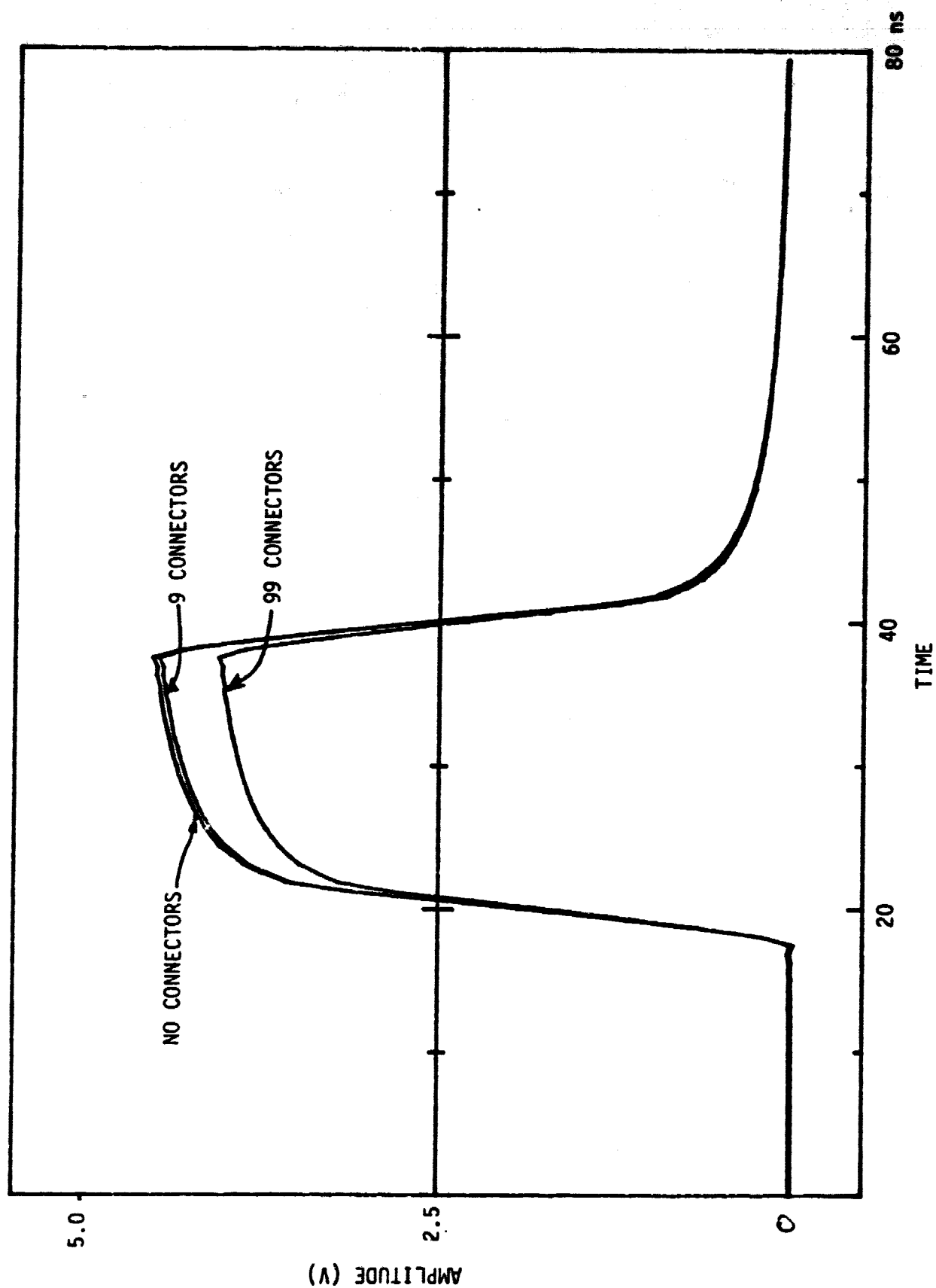


Figure 2. Pulse (Input Rise Time = 3ns).

line. The first two plots are very close to each other which is an indication that the distortion introduced by 9 connectors is negligible. Figure 3 displays the output to a square waveform with 3 ns trapezoidal rise time. Here, only the two cases of 0 and 9 connectors are plotted and the two plots are almost indistinguishable. Figure 4 illustrates the system response to a random pattern. Again the plot for 9 connectors is indistinguishable from the one with 0 connectors. The plot for 99 connectors indicates a significant increase in signal distortion. Figure 5 illustrates the output rise time versus the input rise time. Plot a is obtained using the 30-70% definition while plot b corresponds to the 20-80% definition. Using plot b, 5 ns output rise time is measured when the input rise time is 3.5 ns, while if there were no connectors, the input rise time could be as high as 3.8 ns⁽¹⁾. This means that the appearance of 9 connectors on the line restricts the input rise time by an extra amount of .3 ns which, of course, is small. However, in case of 10-90% definition the change in the input rise time is greater than 1 ns. This last observation is one of the many reasons why 10-90% spec is not suitable for rise time definition.

3. Amplitude Loss

Figure 6 displays the amplitude loss versus the signal asymmetry. Nine connectors are assumed to be present. If Figure 6 is compared with a similar figure in Reference (1), about 1% increase in the amplitude loss becomes apparent. Plot a of Figure 7 displays the line response to a 20 ns pulse while 9 connectors are present. Plot b shows the output if 25% asymmetry is imposed on the pulse. The input rise time is 3 ns.

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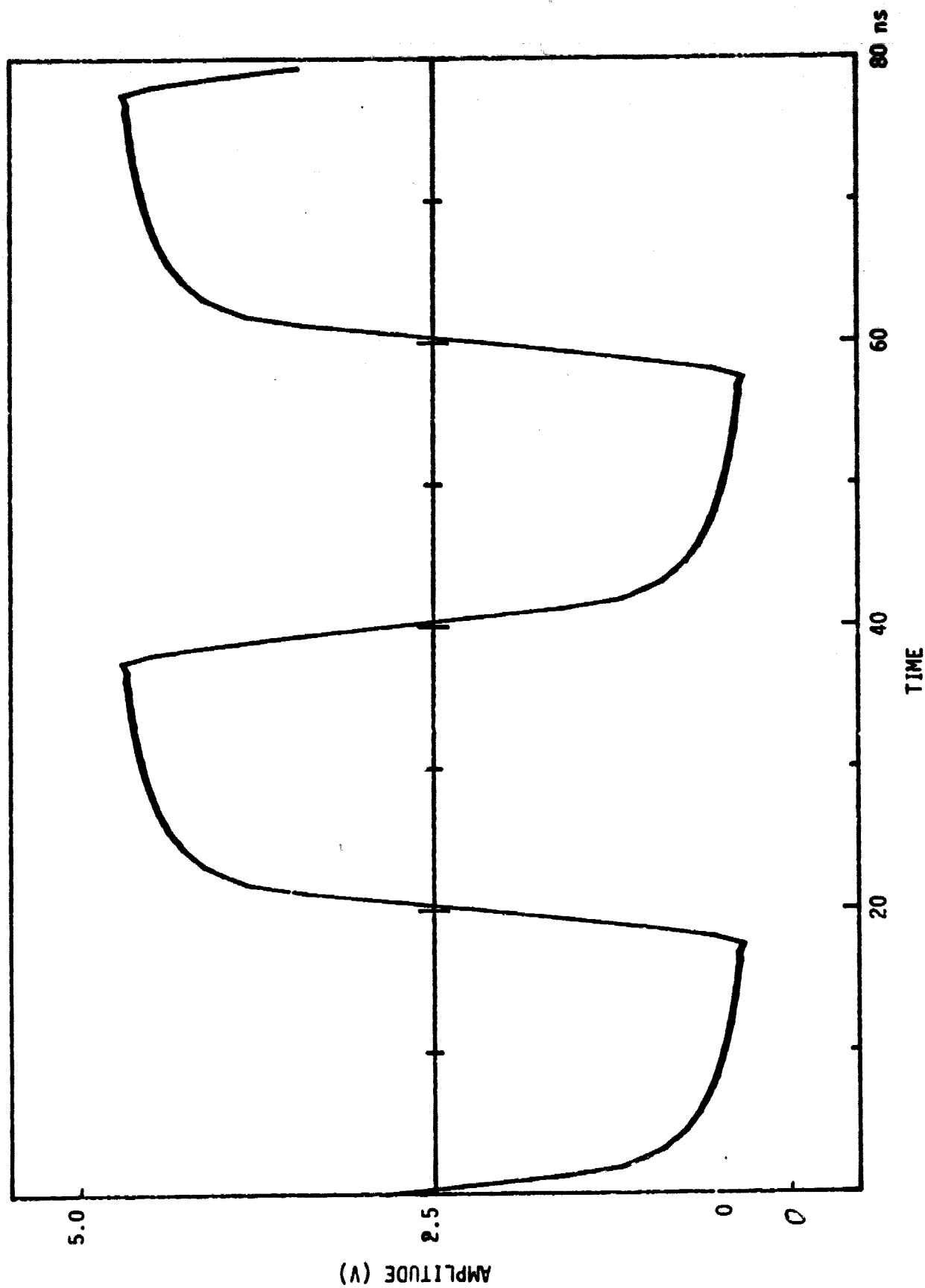


Figure 3. Square Wave (Input Rise Time 3 ns).

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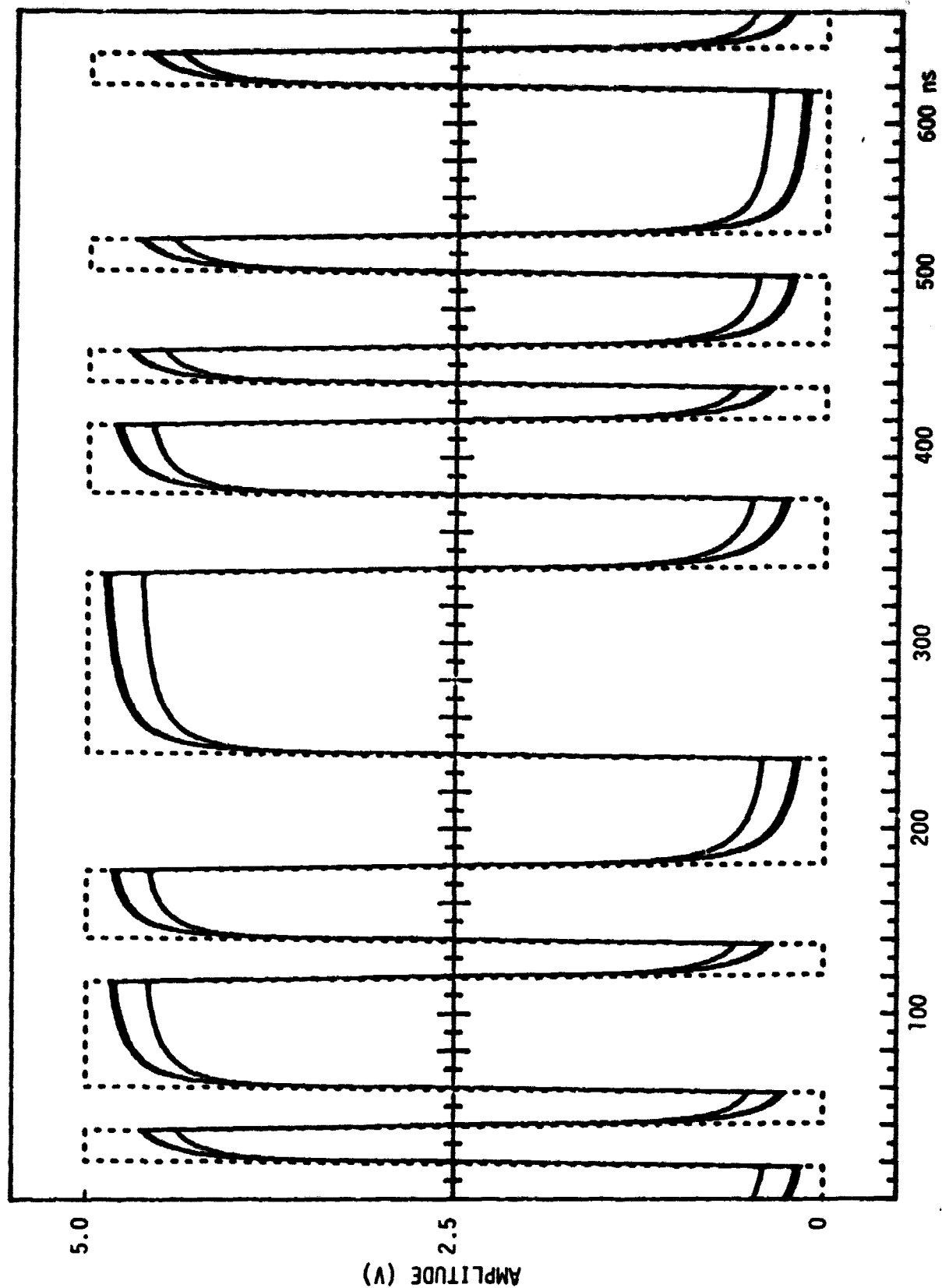


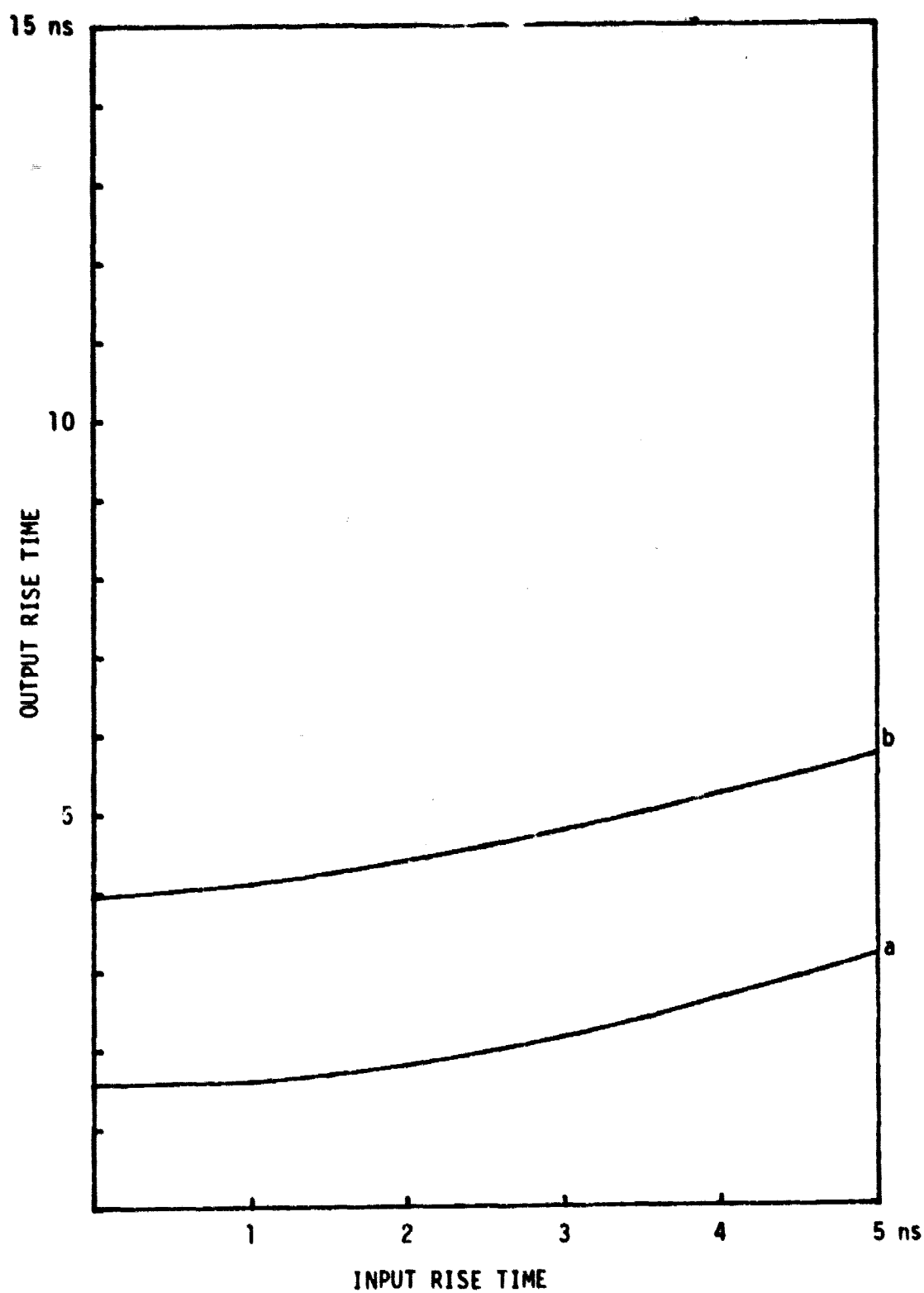
Figure 4. Random Pattern (3 ns Rise Time).

Figure 5.

a: 30-70%

b: 20-80%

9 Connectors on the Line



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Figure 6.

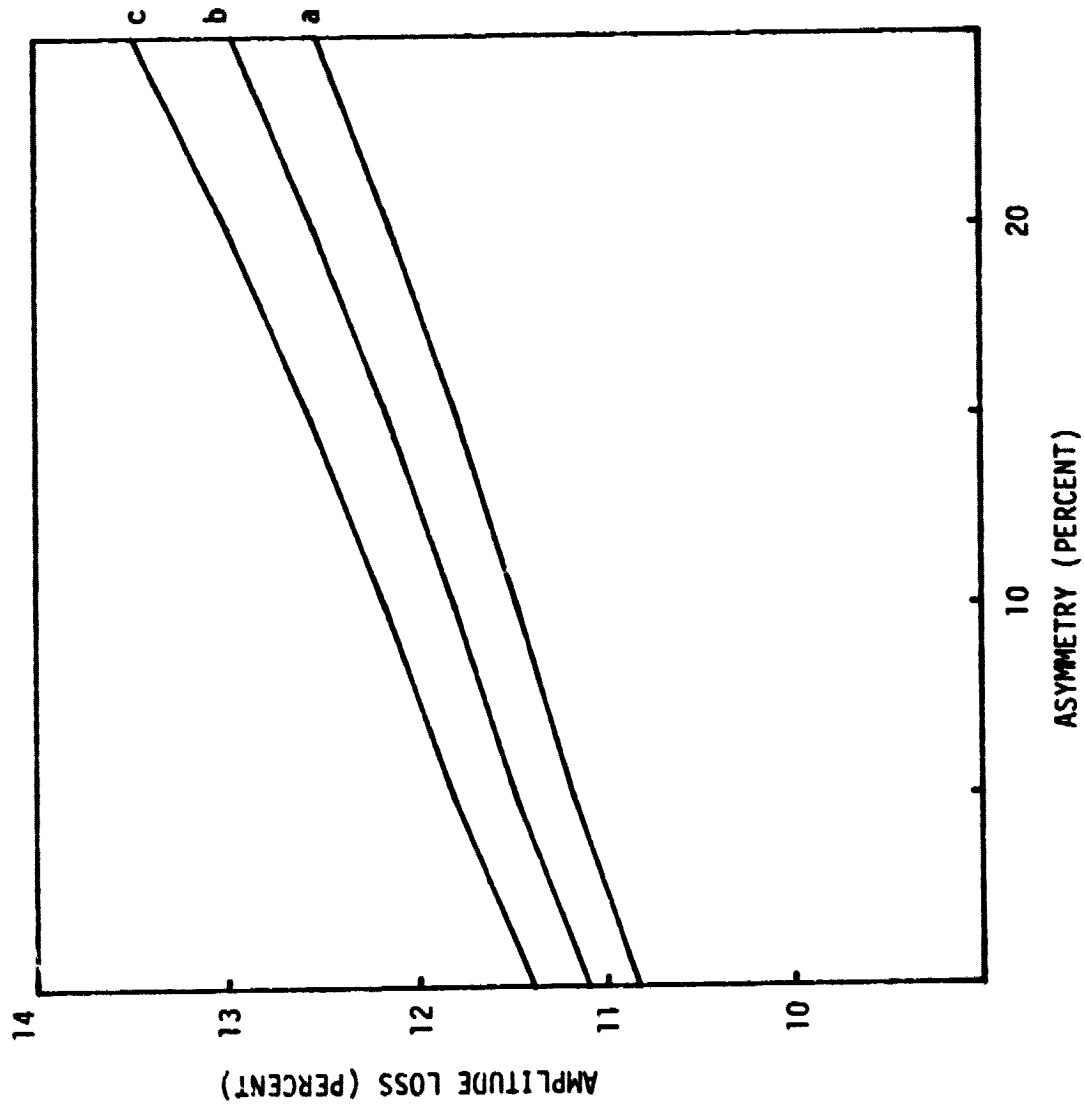
a: 30-70%

b: 20-80%

c: 10-90%

9 Connectors on the Line

3 ns Input Rise Time



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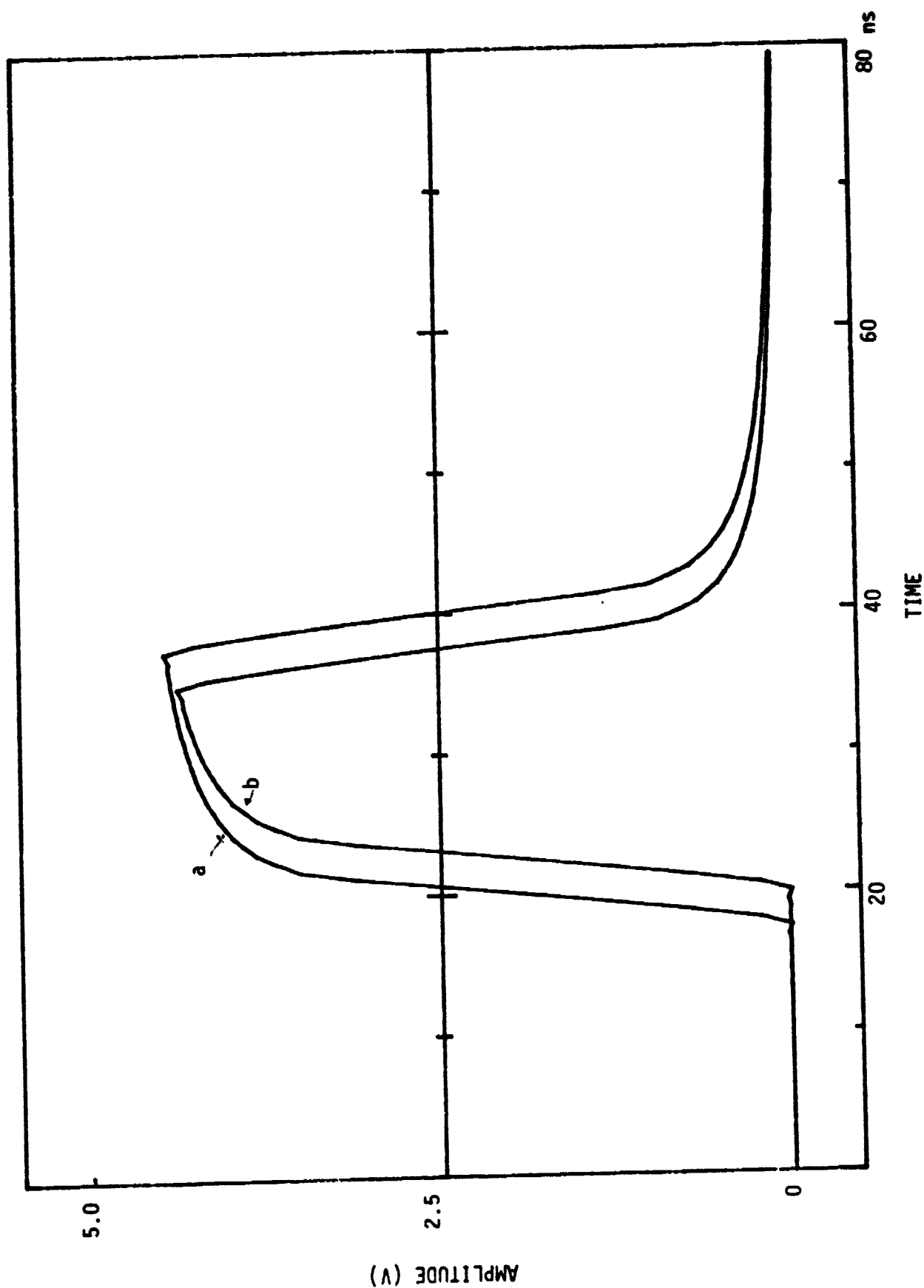


Figure 7.

4. Threshold Variation

Figure 8 displays the timing offset generated by the threshold variations. After comparing this figure to a similar one in Reference (1), the following observation is made. The timing offset is not increased by the presence of 9 connectors when threshold variation is less than 10%. For a variation between 10 and 25%, the offset is increased by a small amount; this increase, however, is not large enough to be of any practical importance (less than .03 ns).

5. Conclusion

This report is a continuation of the work done in Reference (1). The model utilized to represent 100 ft of RG142B cable introduces 2.7 dB amplitude loss at 50 MHz. It is shown that the addition of 9 connectors to the cable at 50 Mbps data rate increases the output degradation by a negligible amount. The threshold variations cause an unwanted time offset at the data reconstruction mechanism output. The following table shows the timing error for two extreme cases. The first case corresponds to a source putting out pulses with .5 volts as the lower level and 6.5 volts as the higher level. The second case coincides with a source putting out -.5 volts and 4.5 volts as two pulse levels. The normal situation is considered to be 0 and 5 volts for the two pulse levels with the threshold set at 2.5 volts. The table also contains the amplitude losses related to the sources under consideration.

Note that the threshold variation is computed in percent so that Figure 8 can always be used. For example, to compute the threshold variation for source 1, number 2.5 is subtracted from 3 (source average) and is divided by the high (6.5) and low (.5) voltage difference (6), and the result is multiplied by 100. Amplitude loss is also represented in

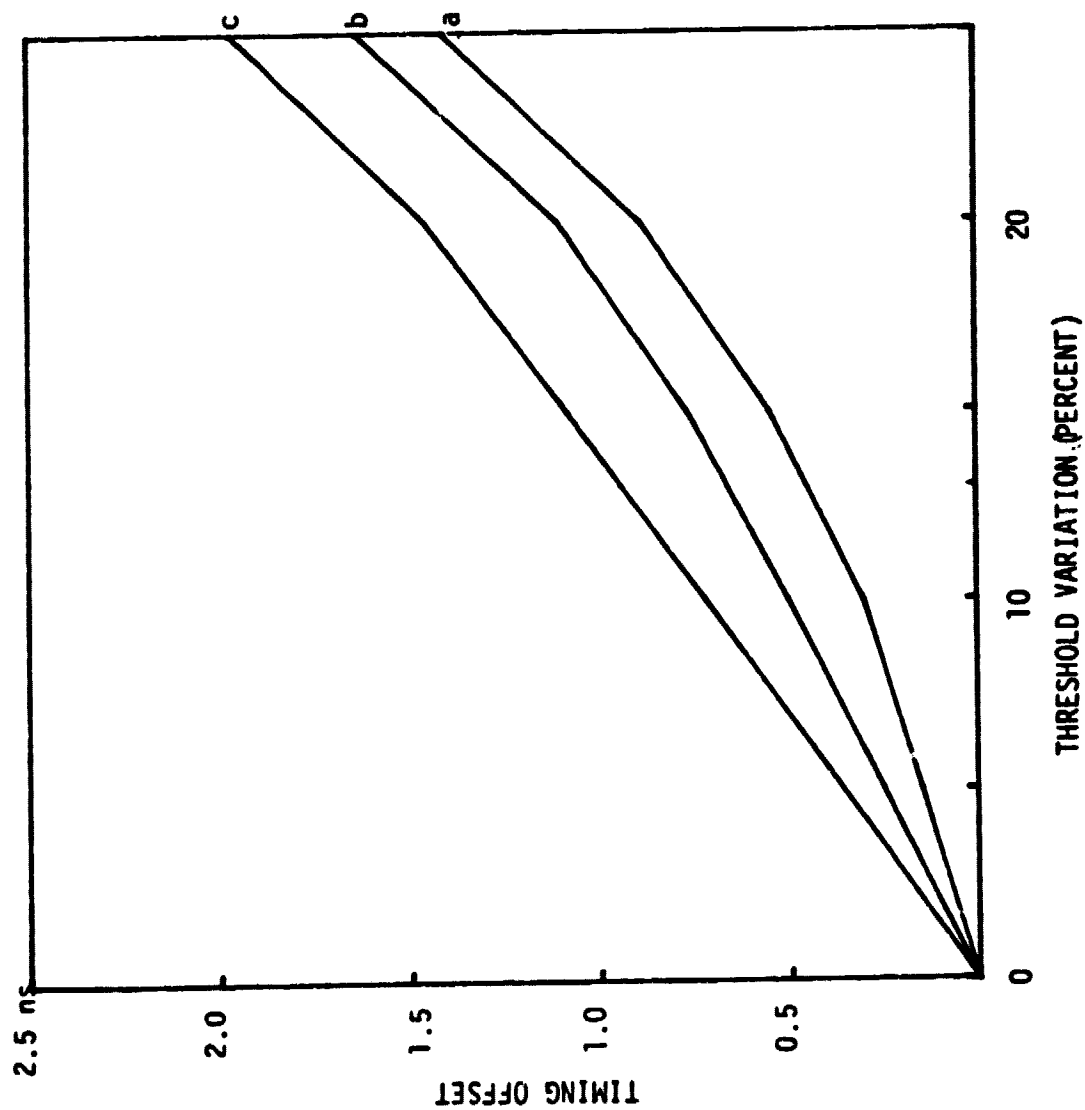
Figure 8 .

a: 30-70%

b: 20-80%

c: 10-90%

9 Connectors on the Line



percent in Figure 6. To convert the amplitude loss to volts the number obtained from Figure 6 is divided by 100 and multiplied by the high and low voltage difference.

Table 1. Source Amplitude Variation (3 ns Input Rise Time).

SOURCE	SOURCE LEVELS IN VOLTS	THRESHOLD VARIATION	TIMING OFFSET	OUTPUT AMPLITUDE LOSS (20% ASYMMETRY)
1	.5-6.5	17%	+.9 ns	.75 volts
2	(-.5)-4.5	10%	-.5 ns	.625 volts

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- [1] "RG142B Coax Cable Response to 50 Mbps Data Input," LinCom Technical Report No. TR-0380-0880, March, 1980.
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- [3] S. Ramo, J. Whinnery and T. Van Duzer, Fields and Waves in Communication Electronics, John Wiley and Sons, New York, 1965, p. 350.
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4.0 ANALYSIS OF MID-BIT CIRCUITRY

Introduction

The uncoded 2 to 50 Mbps data must be corrected for asymmetry before being processed by the convolutional encoder in the Ku-band return link communication subsystem of Space Shuttle Orbiter [1]. This report describes the function of the asymmetry corrector hardware designed by Hughes and also verifies its timing budget. The corrector circuitry is under construction at the present time and is approaching its final phase.

1. Timing Allocation

A total of 5.9 ns is allocated to three major causes of asymmetry:

- a) Source asymmetry T_a defined as the difference between a 1 pulse and a 0 pulse width.
- b) Data rise and fall time contribution due to amplitude loss T_b defined as (20-80% definition for rise time):

$$T_b = \frac{(\text{Amplitude Loss}) \times (\text{Rise Time})}{100 \times .6}$$

- c) Sampling margin reduction due to error in amplitude threshold estimation T_c . Figure 1, copied from Reference [2], can be used to compute this time; for 13% amplitude loss T_c equals 1 ns.

The three timing factors are computed for the worst case of 50 Mbps data 20 ns pulse width. The rise and fall time definition is 20-80% and the rise (and fall) time spec is 6 ns. Amplitude loss (because of the cable) is 13%.

Using the above definitions, time T_b is computed first.

$$T_b = \frac{6 \times 13}{.6} = 1.3 \text{ ns}$$

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Figure 1.

a: 4 ns Rise Time

b: 4.75 ns Rise Time

c: 5.5 ns Rise Time

9 Connectors on the Line

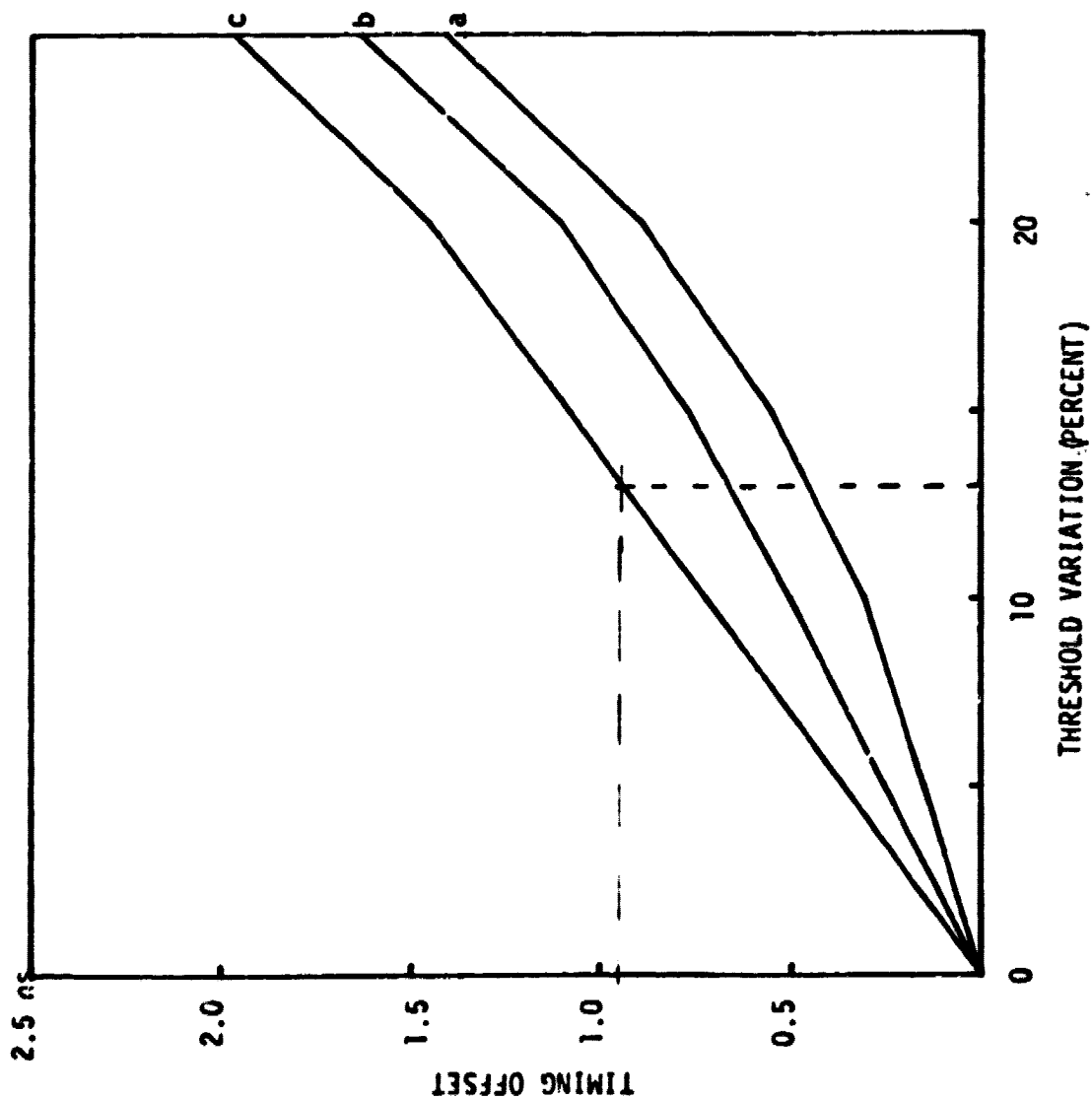


Figure 1 can be used to determine T_c

$$T_c = 1 \text{ ns}$$

To determine the maximum allowable source asymmetry A , T_a must be computed first:

$$T_a = 5.9 - T_b - T_c = 3.6 \text{ ns}$$

Since the pulse width is 20 ns,

$$A = \frac{3.6}{20} \times 100 = 18\%$$

For safety reasons A is selected to be 16%.

Table 1 summarizes all the contributing factors to loss in sampling margin. According to this table the worst case (maximum) loss is 9 ns or 45% ($\frac{9 \times 100}{20}$). The mid-bit corrector hardware functions properly only if loss is below 50%.

To correct for asymmetry a pair of complementary and symmetric clocks, I and Q , are generated, and the data is sampled by the I clock at mid-bit points while the Q clock is made to coincide with the rising edges of the data. Figure 2 illustrates the sampling method on a "10110" data sequence with 40% asymmetry (loss in sampling margin). The method will work only if this asymmetry is below 50%. The concept illustrated in Figure 2 is utilized in asymmetry corrector circuitry. The worst case sampling margin is 5% or 1 ns.

2. Mid-Bit Corrector

The purpose of the Mid-Bit Corrector circuitry of Figure 3 is to generate two complementary clocks, called I and Q , and to position them so that the leading edges of the Q clock coincide with positive-going data transitions, and the leading edges of the I clock can be used to

WORST CASE ERROR-FREE SAMPLING MARGIN
USING HI-LO ADAPTIVE THRESHOLD

CAUSE OF MARGIN REDUCTION	MAGNITUDE
<p style="text-align: center;">SPEC CONTROLLED</p> <p>DATA ASYMMETRY</p> <p>DATA RISE/FALL TIMES PLUS AMPL. LOSS (13%)</p>	<p style="text-align: center;">5.9 NS</p>
<p>THERMAL NOISE</p>	<p style="text-align: center;">± 0.2</p> <p style="text-align: center;">PEAK</p>
<p>PHASE JITTER DATA TO CLOCK</p>	<p style="text-align: center;">± 0.6</p> <p style="text-align: center;">PEAK</p>
<p style="text-align: center;">DESIGN CONTROLLED</p> <p>PLL OUTPUT JITTER</p>	<p style="text-align: center;">± 0.2</p> <p style="text-align: center;">PEAK</p>
<p>RECEIVER PROP DELAY IMBALANCE</p>	<p style="text-align: center;">± 1.0</p>
<p>TOL. OF THRESHOLD LEVEL (±40 MV)</p>	<p style="text-align: center;">± 0.1</p>
<p>MID-CLOCK POSITION RESOLUTION</p>	<p style="text-align: center;">± 0.3</p>
<p>I/Q CLOCK ASYMMETRY</p>	<p style="text-align: center;">± 0.5</p>
<p>SETUP/HOLD TIME DIFFERENTIAL</p>	<p style="text-align: center;">± 0.2</p> <p style="text-align: center;">D/A CONV RESOLUTION ÷ 2 FF FDI, FDQ FF</p>
<p style="text-align: center;">TOTAL</p>	<p style="text-align: center;">± 9 NS</p>
<p style="text-align: center;">LIMIT AT 50 MHZ</p>	<p style="text-align: center;">± 10.0 NS</p>

TABLE 1

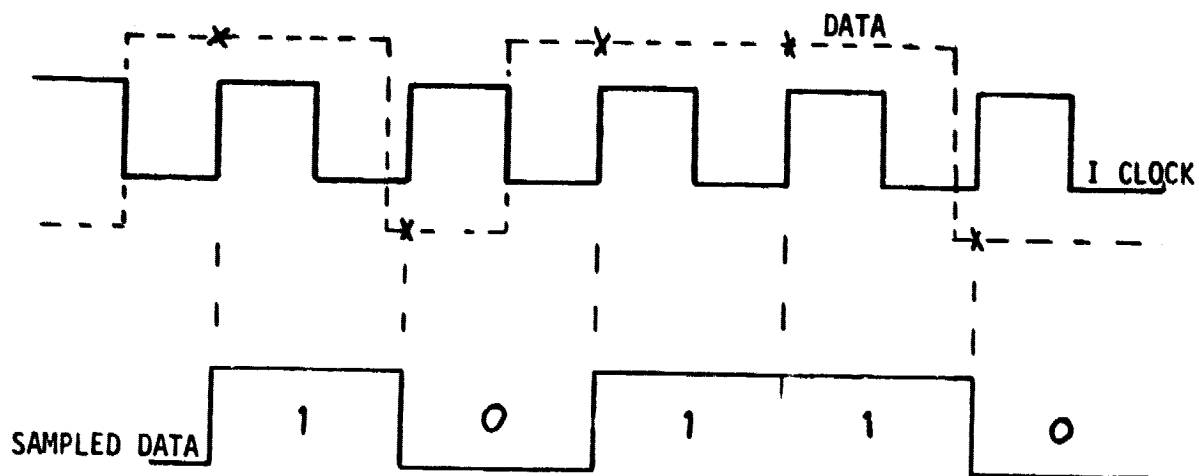
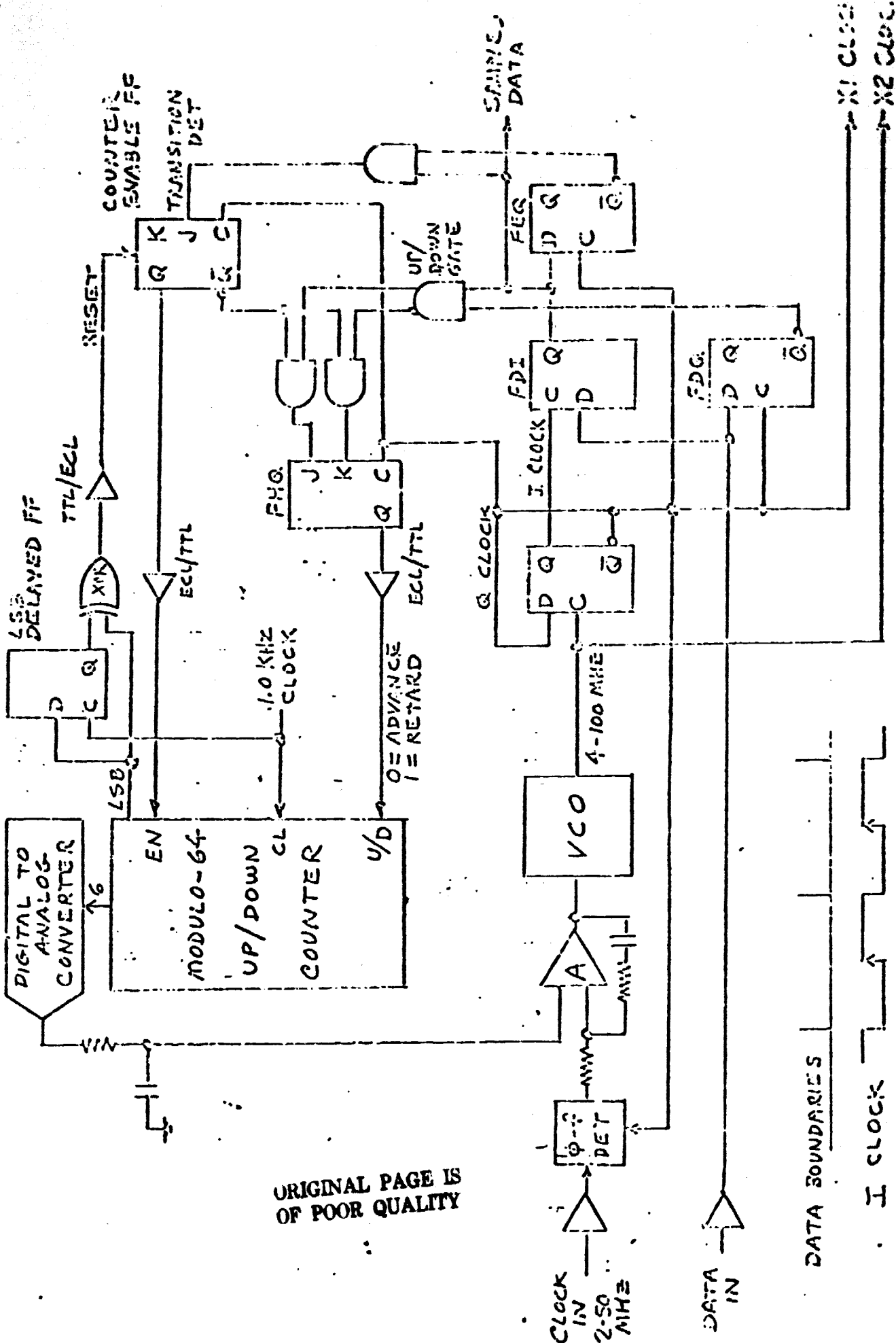


Figure 2. Data Mid-Bit Sampling Using the I Clock.



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Figure 3. Mid-Bit Correlator Block Diagram

reliably sample incoming data. This process is accomplished by injecting a slowly varying dc voltage into the existing phase-lock-loop's voltage control amplifier to adjust the phase of the VCO output relative to data transitions.

The phase-correcting voltage is generated by a six-bit digital-to-analog (D/A) converter. This allows the clock to be phased with respect to the data with a precision of one part in 64 (six-bit resolution). This precision is equivalent to 5.6 degrees (360/64).

The principal components of the corrector circuitry are the phase-lock-loop components (phase-frequency detector, amplifier, voltage-controlled oscillator (VCO), and divide-by-two flip-flop); the six-bit D/A converter; a modulo-64 up/down counter; and logic to detect clock/data skew.

The voltage level out of the D/A converter is controlled by the state of the modulo-64 up/down counter. The counter is clocked by a 1.0 KHz clock, but it is prevented from being incremented at more than a 2.0 millisecond rate by external logic. This timing, shown in Figure 4, allows the phase-lock-loop to settle from a D/A voltage change for one millisecond before the next clock/data phase comparison is permitted. The logic works as follows:

The counter will be incremented by alternate 1.0 KHz clocks if a positive-going data transition has occurred during the previous one millisecond time period, which is indicated by the true state of the counter enable flip-flop. During the one millisecond period after each counter update, the counter enable flip-flop is held reset by an exclusive-OR gate that detects that the counter's least significant bit (LSB) has just changed. As shown, the LSB output is delayed for one

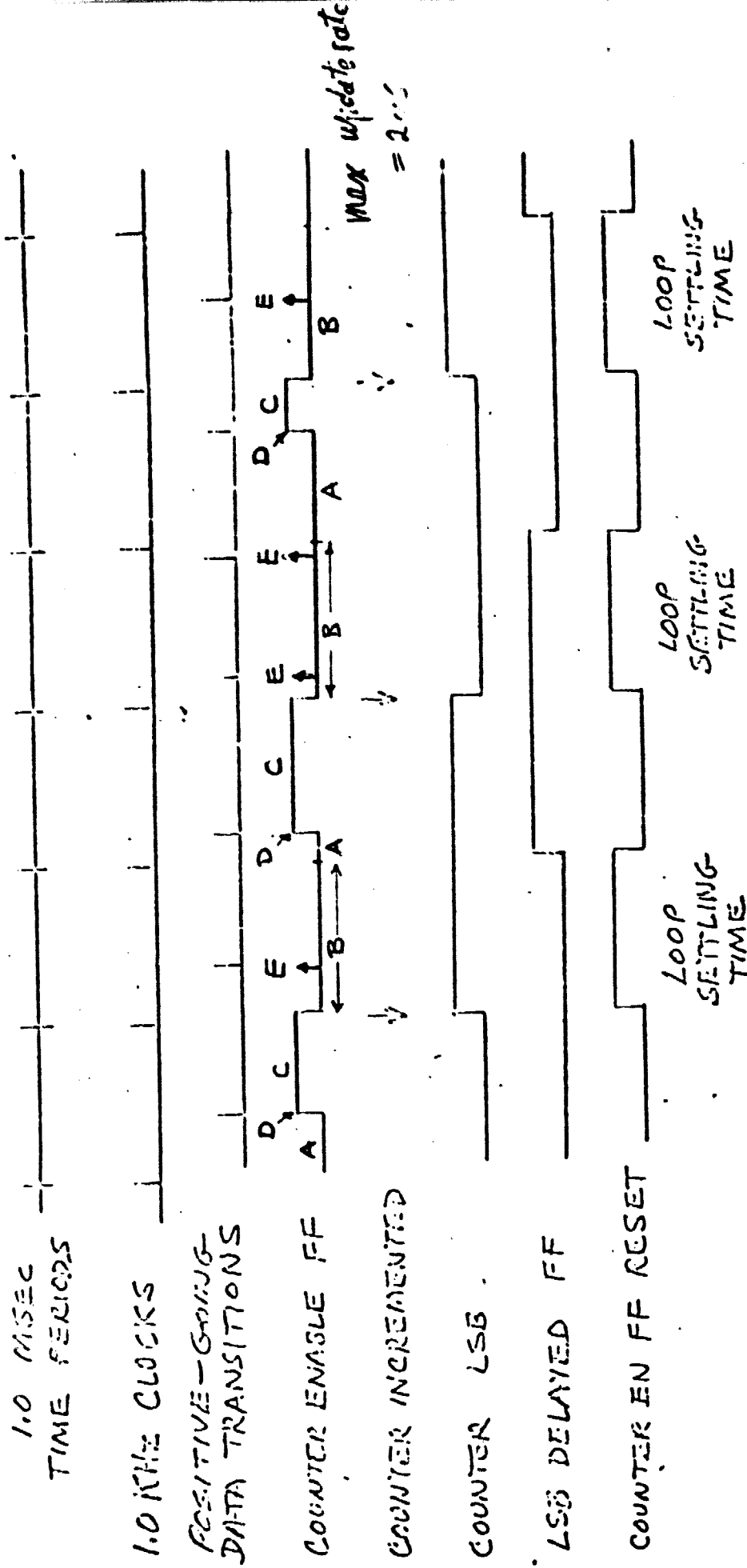


Figure 4. Modulo-64 Up/Down Counter Timing.

millisecond through the LSB delayed FF, the output of which is exclusively ORed with the LSB output to produce the loop-setting time interval.

Figure 5 shows the state diagram of the counter enable flip-flop. States D and E are unstable. Starting from state A, upon arrival of a data transition, a switch to state D occurs. Since D is unstable, the flip-flop automatically moves to state C. State C is terminated when a 1 KHz clock transmission occurs. The next state B lasts 1 ms until another 1 KHz clock transmission (positive) arrives. This will put the flip-flop back into the original state A. While at state B, it is conceivable that because of occurrence of data transitions this state would temporarily switch onto state E. However, since E is unstable it will immediately change to state B. This phenomenon can also happen between states C and D.

The flip-flop which divides the VCO output frequency by two produces complementary I and Q clock outputs, as shown in Figure 6. Incoming data is clocked into flip-flop FDI by the mid-bit I clock, then delayed a half-bit time through FEQ, clocked by the Q clock. Whenever a data transition occurs, the two flip-flops will become out of phase for half a bit time. An AND gate detects positive-going transitions which are clocked into the counter enable flip-flop by the Q clock provided the reset pulse generated during the loop-setting interval is not present. Thus, the first positive transition after the reset pulse disappears will cause the counter enable flip-flop to be set.

To determine if the phase of the VCO clock should be advanced or retarded, data is clocked into flip-flop FDQ by the Q clock. If transitions occur early (solid lines in Figure 6), FDQ will change a half bit time before FDI. If transitions are late (dotted lines in Figure 6),

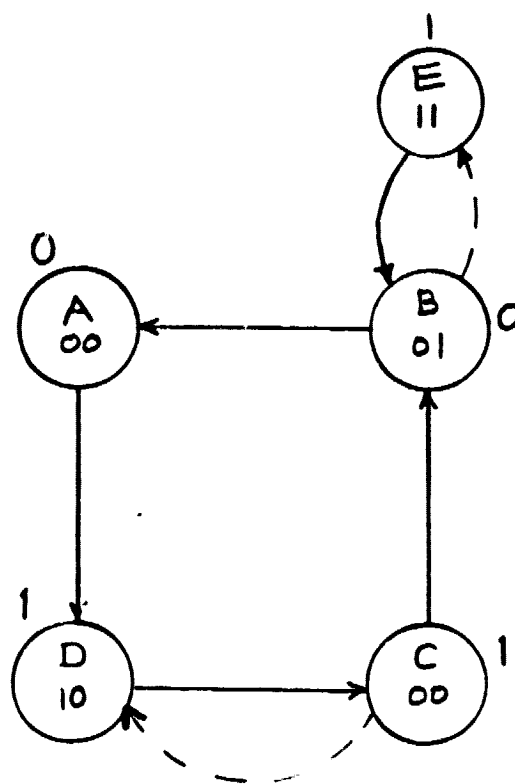


Figure 5. Counter Enable Flip-Flop State Diagram.

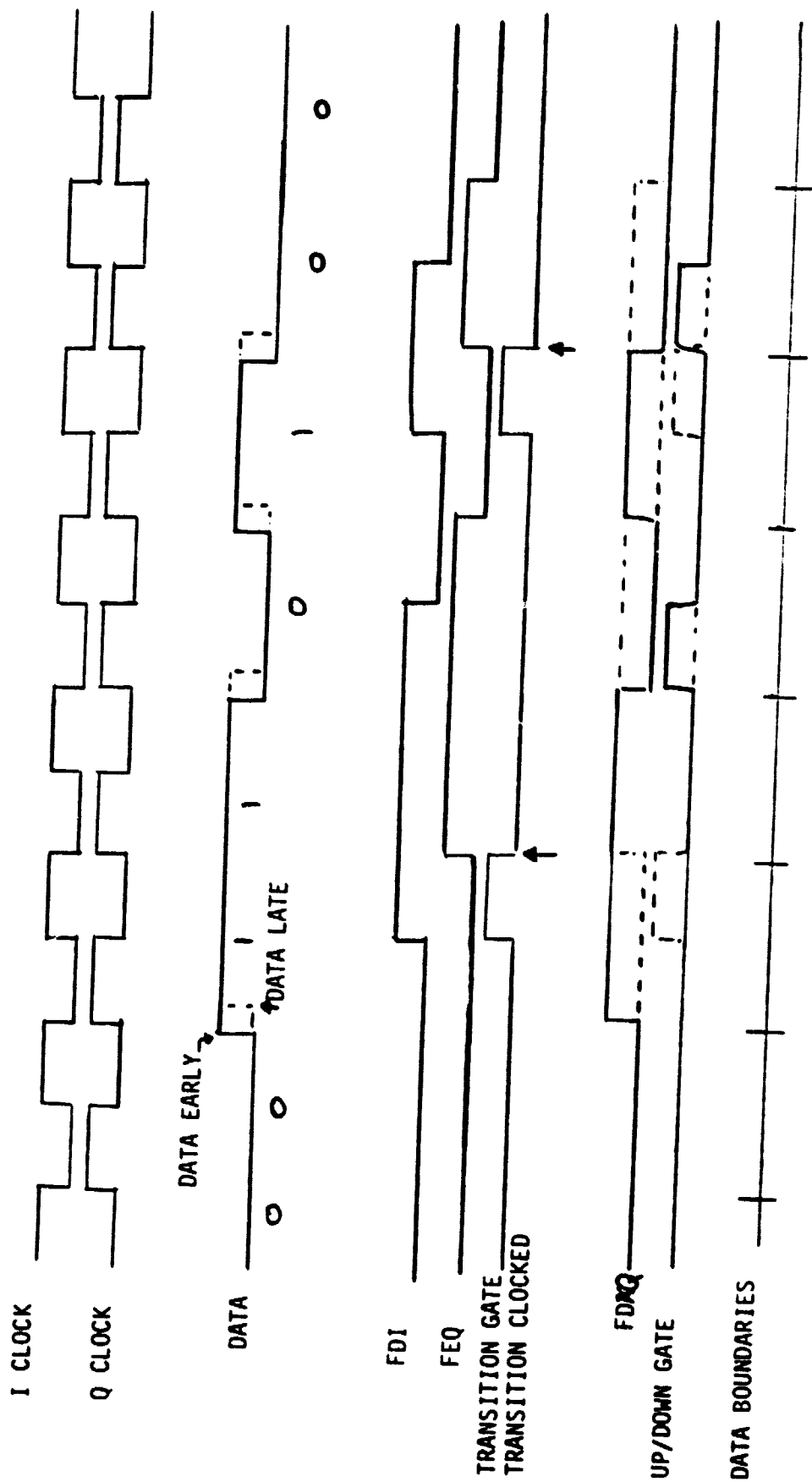


Figure 6. Mid-Bit Corrector Timing.

FDQ will change a half bit time after FDI. This phasing of FDQ and FDI is compared in the Up/down AND gate. A logic zero at Q clock time calls for a clock phase advance; a logic one, a phase delay.

The state of the up/down gate at Q clock time is monitored by flip-flop FHQ. When a positive transition is detected by the counter enable flip-flop, the latest up/down gate information will be stored in FHQ and preserved against subsequent changes by the counter enable flip-flop output state which changes at Q clock time. The true state of the counter enable flip-flop allows the up/down counter to be incremented by the next 1.0 KHz clock; the state of FHQ controls whether the count is advanced or retarded.

After the loop achieves the correct clock/data phasing, the counter will alternate between an up command and a down command on successive updates. When a new set of clock and data channels is selected, a maximum of 31 new counts could conceivably be required by the counter before proper phasing is achieved. If data transitions occur as often as two in any one-millisecond time period, the loop will acquire proper phasing within 62 millisecond when 31 counts are required.

Data sampled by flip-flop FDI will be used by the Convolutional Encoder logic. For mid-bit sampling of this data, the Q clock will be supplied, along with the X2 clock.

To reduce power and parts count, only that portion of the mid-bit corrector circuitry that must operate at megahertz frequencies has been implemented by ECL parts. The low-speed up/down counter, for example, will be mechanized by low-power TTL circuits, with level shifters being used between different logic levels.

3. Threshold Estimation and the Data Receiver

The purpose of the circuit at the upper left corner of Figure 7 is to reconstruct sharp bit pulses from degraded input waveform. Figure 8 displays a PN sequence after traveling through 100 ft of coaxial cable. To recover the original pulse shape, it is necessary to establish a threshold to differentiate between the zeros and the ones of the sequence. To generate the proper threshold, the circuit detects the high and the low peaks of the waveform and forms the average of these two quantities. The .1 F capacitor preceded by a diode responds quickly to the proper peak and obtains the peak value. The buffer saves the peak voltage for at least 1 ms. When a new source is selected the high peak might drop as much as 2 volts (Table 2). The circuit is relatively slow in responding to sudden high peak drops; according to Mr. Pfiffner of Hughes it takes the circuit 350 ms to respond to a drop of 2 volts. This observation is illustrated in Figure 9.

Assuming an RC model, the time constant of this circuit can be computed as follows. Again, observing that 350 ms is needed to drop from 6.5 to 4.5 volts and calling the time constant τ

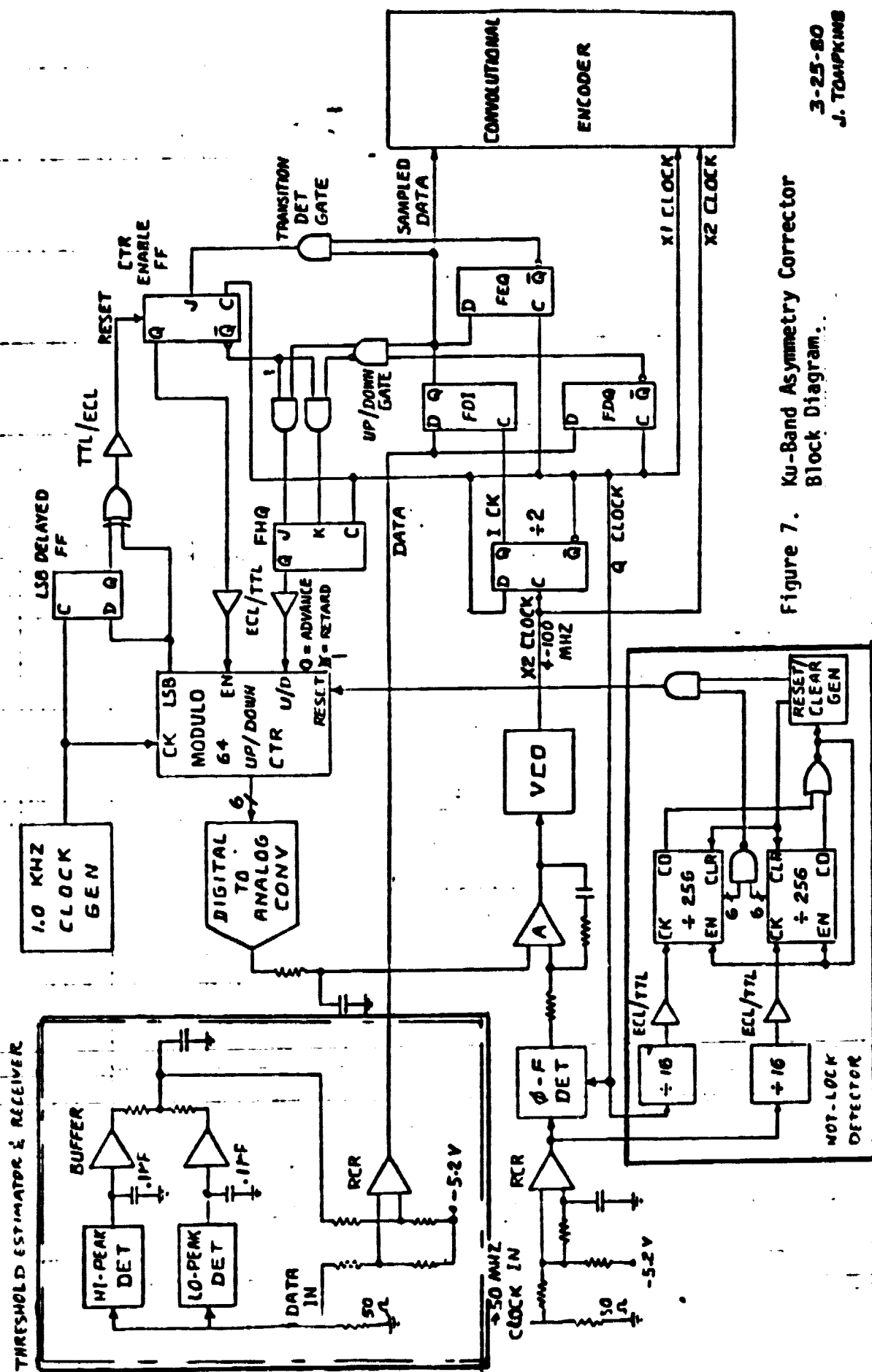
$$\frac{6.5}{4.5} = e^{.35/\tau}$$

or $\tau = 1$. With such a high time constant, the voltage change in 1 ms is negligible.

4. False Lock

In the transient period of frequency acquisition, the phase-locked loop tracking the input clock in the asymmetry corrector may false lock if the dc voltage injected into the voltage-controlled amplifier is

ASYMMETRY CORRECTOR BLOCK DIAGRAM



3-25-80
J. TAMPKINS

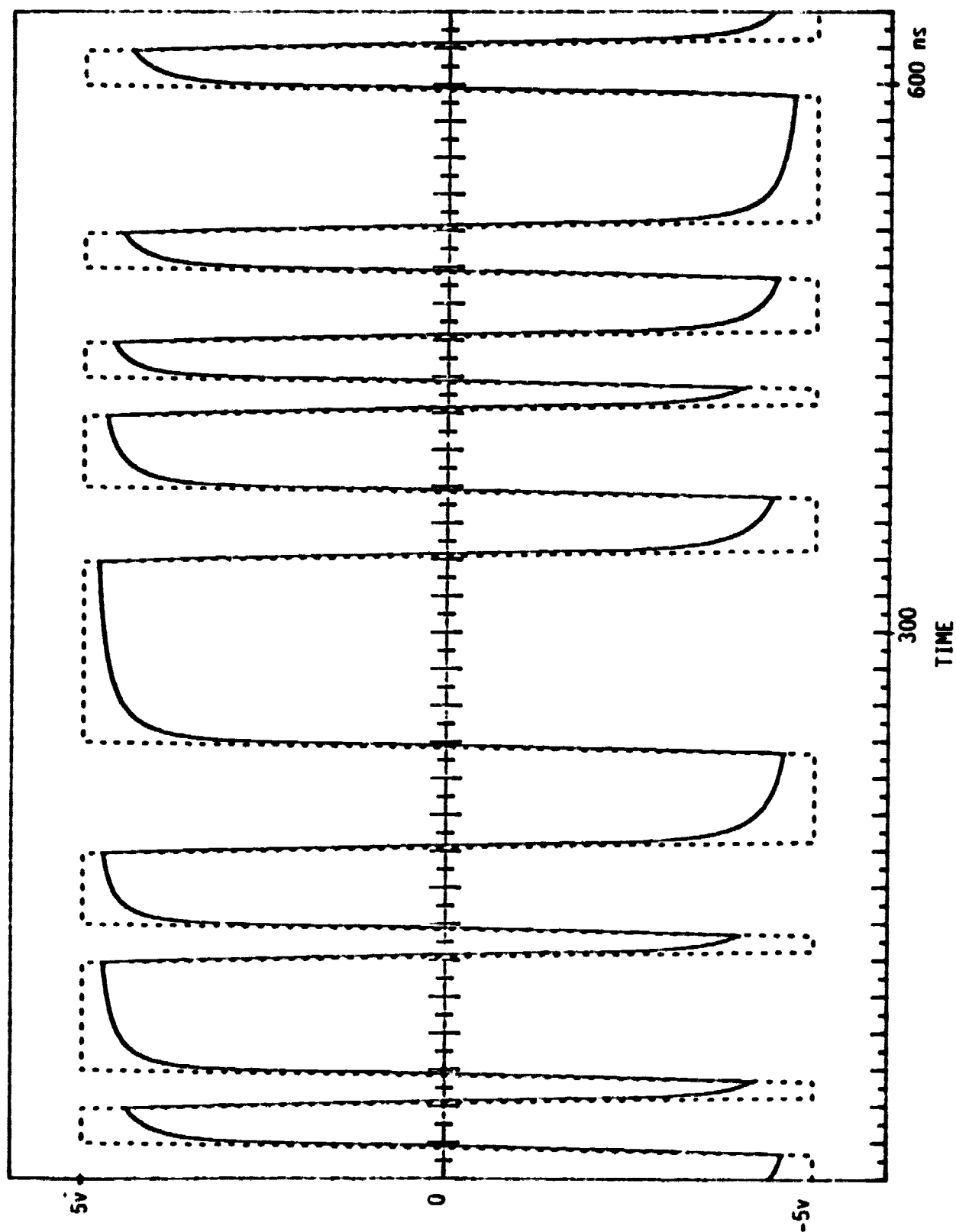


Figure 8. PII Sequence 0101101100011101001101001000010;

LOGIC 1	MAX	6.5
	MIN	4.5
LOGIC 0	MAX	.5
	MIN	-.5

Table 2. Source High and Low Peaks

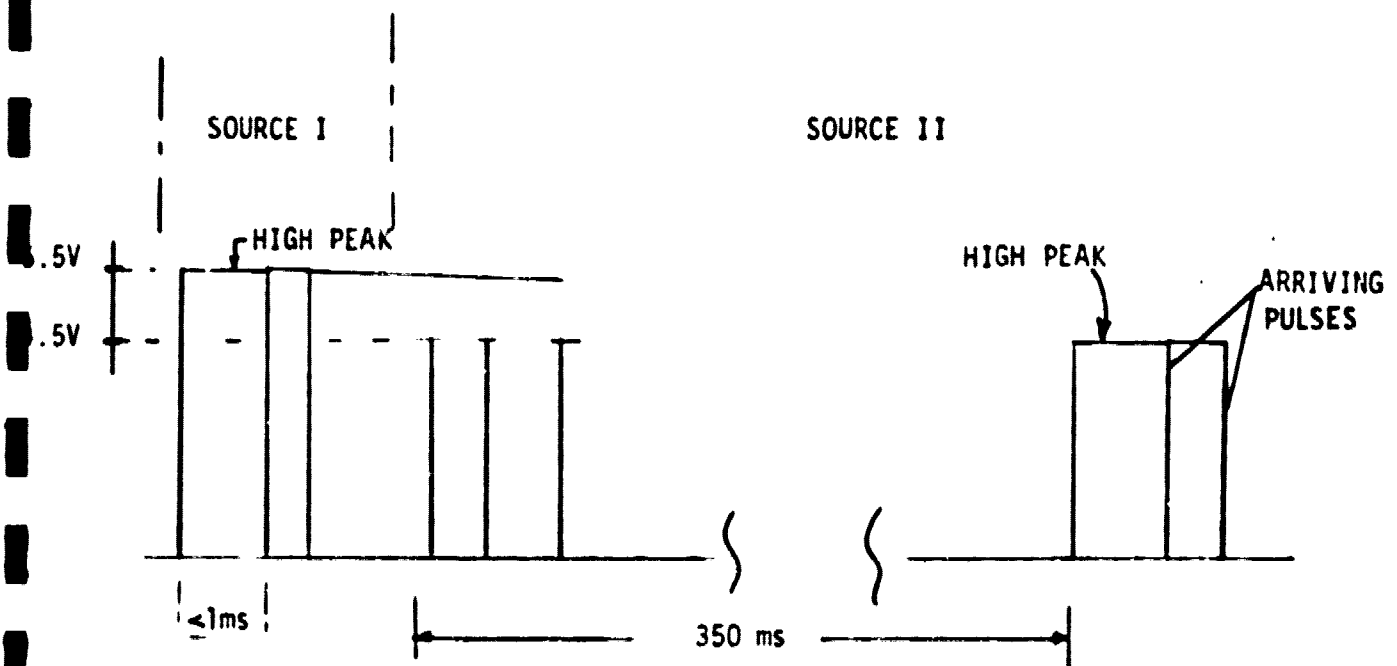


Figure 9. High Peak Detection When Source Amplitude Drops 2 Volts. The Equivalent RC Circuit Time Constant = 1.

not equal to zero. To avoid false lock, the circuit at the lower left corner of Figure 7 is used to reset the up/down counter to zero every time the clock frequency changes. The circuit operates on this principle that at the end of every 256 counts if any of the six most significant bits of the modulo 256 counters is not a one the up/down counter is automatically reset. This condition can only happen if the two frequencies of the input clock and a clock are at least 1.67%(100/64) apart. For example, if Q clock frequency is 40 MHz and the input frequency is larger than 40.7MHz this circuitry will reset the up/down counter. For frequency changes smaller than 1.6%, the phase-locked loop automatically corrects the phase, hence there is no need to reset the up/down counter. The time required for the circuit to detect a not-in-lock situation can be computed. It is clear that 4096 pulses are required before the up/down counter can be reset. In the vicinity of 2 MHz, this time equals 2 ms; while at 50 MHz it is much shorter and equals .08 ms.

5. Acquisition

The acquisition process is basically composed of two parts: frequency and phase acquisitions. Figure 10a illustrates the block diagram of the phased-locked loop. The phase-frequency detector can operate either in a frequency detection (when frequencies are unequal) or in a phase detection (when frequencies are equal) mode. Figure 10b shows the approximate frequency detector characteristic while Figure 10c illustrates the phase detector characteristic. Frequency detector characteristic is only valid if frequencies f_1 and f_2/N of Figure 10a are not equal.

5.1 Frequency Acquisition Time

The differential equation describing the loop behavior in the frequency acquisitions mode is

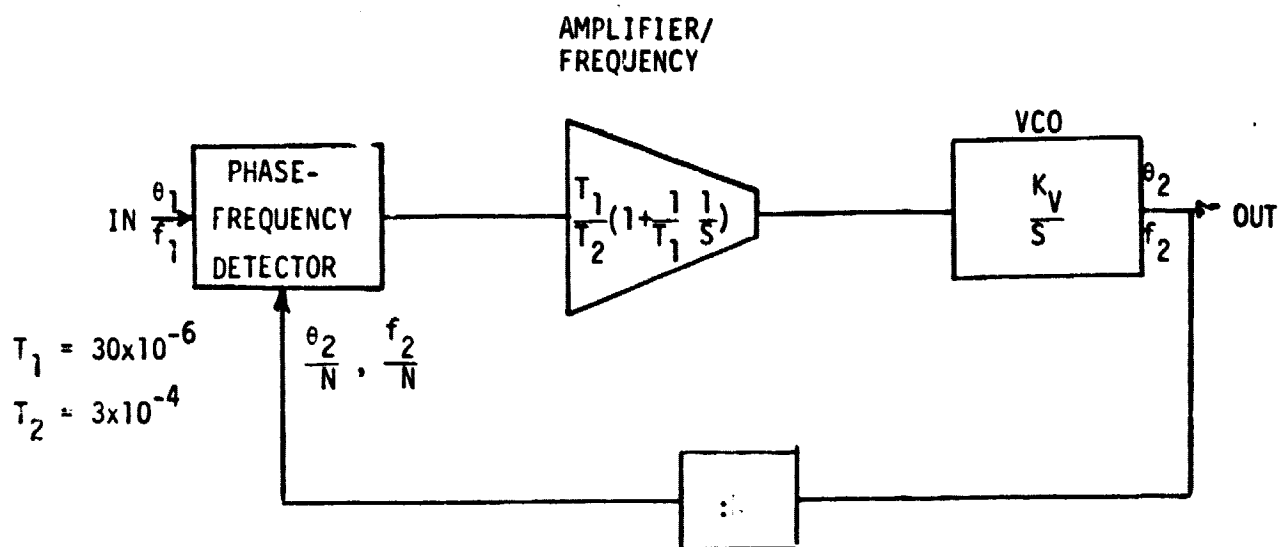


Figure 10a. Phase-Locked Loop.

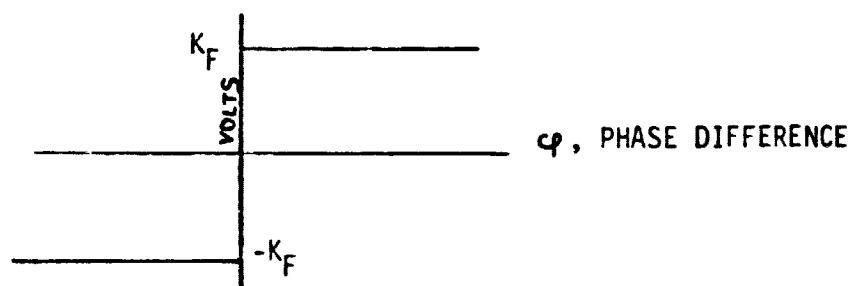


Figure 10b. Frequency Detector Characteristic.
 $\varphi \neq 0$

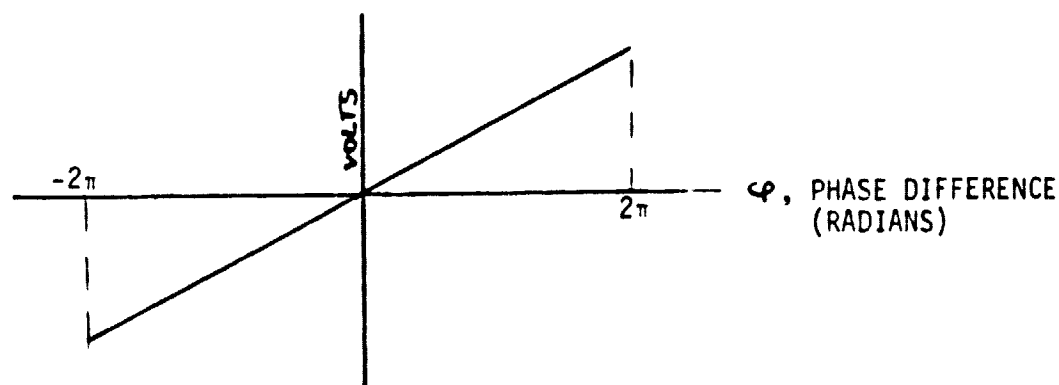


Figure 10c. Phase Detector Characteristic.

$$\ddot{\varphi} + \frac{K_F K_V}{N T_2} = 0 \quad \varphi > 0 \quad (1)$$

$$\ddot{\varphi} - \frac{K_F K_V}{N T_2} = 0 \quad \varphi < 0$$

where φ is the (nonzero) phase error $\theta_1 - \theta_2/N$, K_F is a constant in volts that depends on the frequency detector, K_V is the VCO gain, T_2 is a constant parameter of the loop filter, and N is equal to 2. Assuming the initial phase is θ_0 and initial frequency offset is $\Delta\omega/2\pi$, the first (or second) equation in (1) can be used to determine $\varphi(t)$.

$$\varphi(t) = \theta_0 + \left(\Delta\omega - \frac{K_F K_V T_1}{2T_2} \right) t - \frac{K_F K_V}{4T_2} t^2 \quad \varphi > 0 \quad (2)$$

The frequency acquisition time T_{acq} can be computed by setting the derivative of $\varphi(t)$ equal to zero.

$$\varphi(t) = \Delta\omega - \frac{K_F K_V T_1}{2T_2} - \frac{K_F K_V}{2T_2} T_{acq} = 0 \quad (3)$$

Thus

$$T_{acq} = \frac{\Delta\omega - \frac{K_F K_V T_1}{2T_2}}{\frac{K_F K_V}{2T_2}} \quad (4)$$

Since $K_F K_V T_1/T_2$ is small, equation (4) can be simplified to

$$T_{acq} = \frac{\Delta\omega}{\frac{K_F K_V}{2T_2}} \quad (5)$$

Consulting Motorola MC12040 and MC1658 data sheets, typical values of K_F and K_V can be found.

$$K_F = .35 \text{ volts}$$

$$K_V = 45 \times 10^6 \text{ rad/s/v}$$

$$\frac{K_F K_V}{2T_2} = 16.5 \times 10^{10}$$

Figure 11 illustrates $\phi(t)$ for maximum frequency offset of 50 MHz. T_{acq} can be computed either using equation (5) or Figure 11. The computed value for T_{acq} is approximately 1.9 ms. Thus, frequency acquisition occurs in a relatively short time.

5.2 Phase Acquisition Time

The linear characteristic function of the phase detector is illustrated in Figure 10c, and the linear loop equation is

$$\ddot{\phi} + \frac{K_\phi K_V T_1}{2T_2} \dot{\phi} + \frac{K_\phi K_V}{T_2} \phi = 0 \quad (7)$$

where K_ϕ is the phase detector gain in volts/rad. Defining $\omega_n = \sqrt{K_\phi K_V / 2T_2}$ and $\zeta = \frac{T_1}{2}$, equation (7) simplifies to

$$\ddot{\phi} + 2\omega_n \zeta \dot{\phi} + \omega_n^2 \phi = 0 \quad (8)$$

Assuming $K_\phi = .111 \text{ v/rad}$ and using the data given earlier in this section, ω_n and ζ can be computed:

$$\omega_n = 2.29 \times 10^5$$

$$\zeta = 3.44$$

Solving the second order differential equation(8):

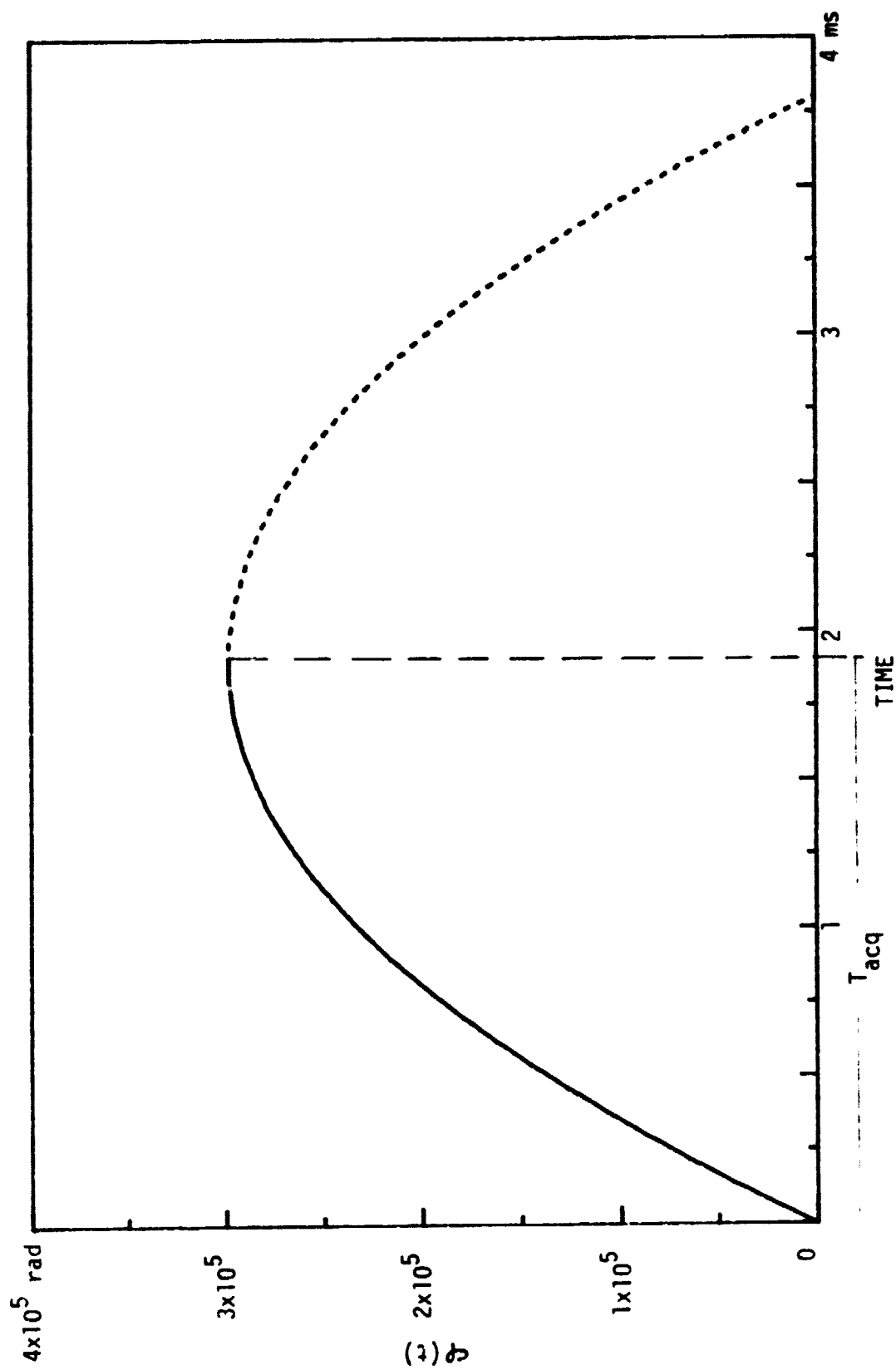


Figure 11. Phase Error $\phi(t)$ Due to a Step in Frequency $(\Delta\omega/2\pi)$; $\Delta\omega = 2\pi \times 50 \times 10^6$

$$\varphi(t) = c_1 e^{-.344tx10^5} + c_2 e^{-15.4tx10^5} \quad (9)$$

where c_1 and c_2 depend on the initial conditions:

$$\varphi(0) = \theta_0$$

$$\dot{\varphi}(0) = \Delta\omega - 2\omega_n \zeta \theta_0$$

Figure 12 illustrates $\varphi(t)$ as a function of $\omega_n t$. From this figure one can conclude that phase is acquired in less than 1 ms. For example if $\Delta\omega = 0$, the phase $\varphi(t)$ becomes less than .5 degree in just .1 ms.

After the clock frequency and phase are acquired, the modulo 64 counter will function as a slow phase corrector to synchronize the Q clock with the data. The counter assumes one out of 64 possible states, and the rate of change is 2 ms. Since a maximum of 31 counts are required to acquire a worst case initial phase error of 180° , the loop will achieve proper phasing within 62 ms (assuming at least two data transitions per millisecond).

5.3 Total Acquisition Time

Table 3 summarizes all the timing factors involved in acquiring a new set of data/clock input.

	Max Time Requirement in MS
Threshold Estimation	350
No-In-Lock Detection	2
Frequency Acquisition	2
Phase Acquisition	1
Clock and Data Sync	62

Table 3.

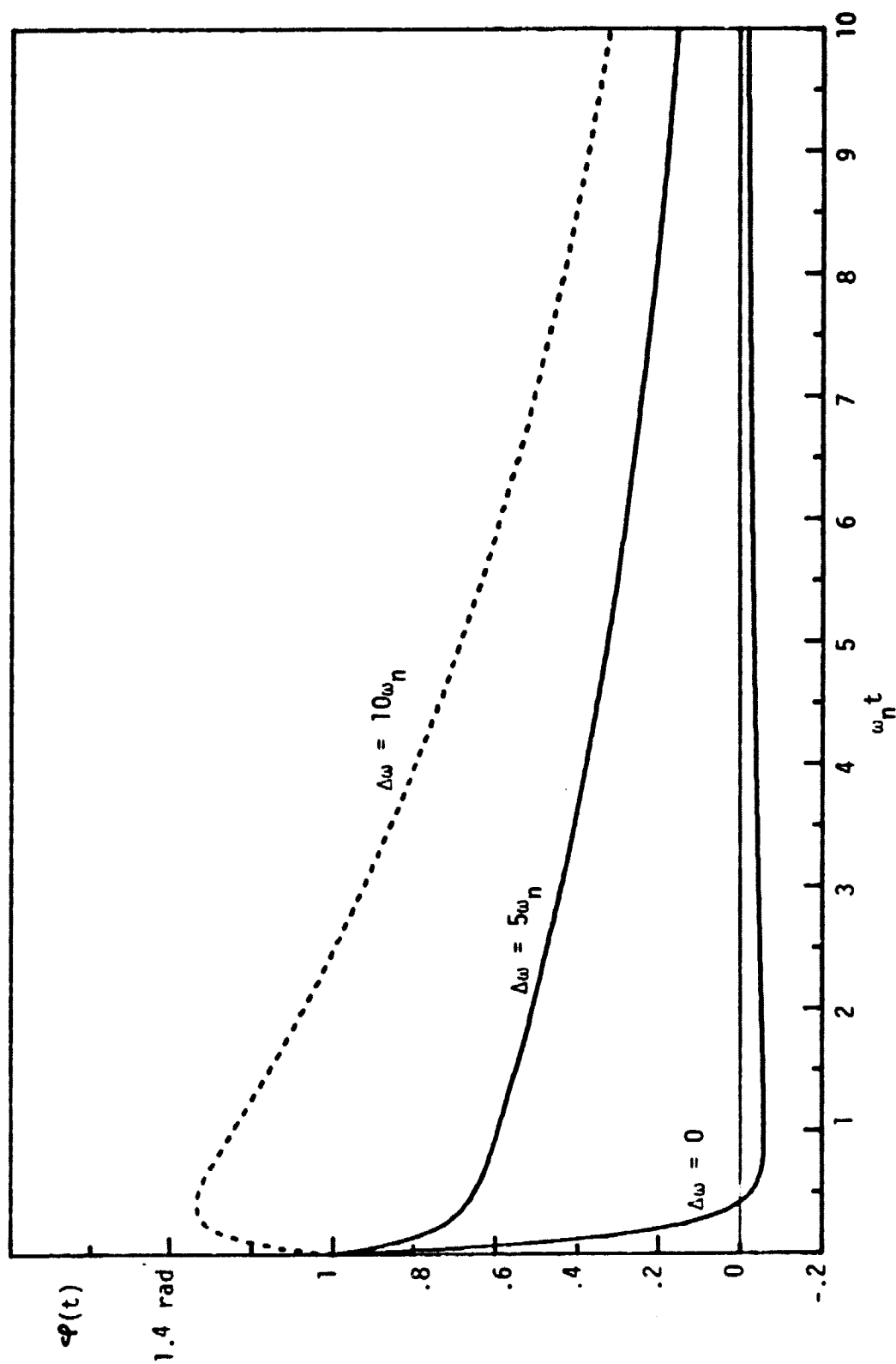


Figure 12. Phase Error $\phi(t)$ Due to Initial Phase of 1 rad and Frequency Step of $\Delta\omega/2\pi$; $\omega_n = 2.92 \times 10^5$, $\xi=3.44$.

Since the threshold estimation and other acquisition operations can happen simultaneously, it seems a total of 350 ms would be adequate. Yet, for safety reasons, a total acquisition period of 400 ms is suggested.

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2. "RG142B Coax Cable Response to 50 Mbps Data Input," LinCom Corporation Technical Report No. TR-3080-0880, March 1980.
3. "RG142B Cable Response to 50 Mbps Data Stream in the Presence of Coaxial Connectors," LinCom Corporation Technical Report No. TR-0480-0880, April 1980.

LINCOM MEMO

To: Don Pusch

Date: June 9, 1980

From: C. M. Chie and W. C. Lindsey

Subject: GPS Constellation Conference at SAMSO, June 5, 1980

cc: J. MacLeod, B. Batson, J. Johnson, W. Teasdale

Abstract

The purpose of the GPS Constellation Conference is to address the budget-driven program change to reduce the number of satellites from 24 to 18 in the GPS network. Its impact on the Space Shuttle program in terms of Shuttle mission schedules and Shuttle navigation via GPS are summarized.

Current GPS Status

The conversion of the GPS program from concept validation to full scale engineering development was approved by DESARK II in 24 June 1979. Two user set contracts were awarded to Magnavox and Rockwell Collins from which one will be selected. Another contract was awarded to Rockwell International last summer for satellite replenishment. The control segment contract will be awarded in September of this year. Currently there are six space vehicles (SV) on orbit and 4 of them are functioning up to specification while the two earlier ones have clock problems.

Last Christmas, a reduction from 24 to 18 SV in the GPS network was directed by OSD as a result of budget cuts. The decision from 24 to 18 is strictly a cost-saving measure and OSD was aware that a constellation of 18 SV is neither optimal nor desirable to support civilian and military requirements.

Shuttle Launch Schedules

All 18 SV will be launched by the Space Shuttle either during shared and/or dedicated missions. This will occur during the time-frame from late 1984/early 1985 to 1987. In 1987, GPS will be fully operational. Each launch will carry 2 to 3 satellites depending on the constellation selected and whether the Shuttle is shared.

Shuttle Navigation via GPS

The plan now is to keep 5 functional SV until 1984 when the first Shuttle launch is scheduled. The new SV will be added in such a fashion so as to optimize world-wide coverage percentage. The ultimate goal is to select a satellite constellation that allows and maximizes 3-D continuous world-wide coverage when GPS is fully operational. A degradation of performance in the form of isolated "outage" pockets where the navigation accuracy is unacceptable is anticipated from the reduction of the number of satellites (see next section for more detail). For a number of users the exact location of these pockets is more important than the total percentage of world-wide coverage. For example, the Space Shuttle may need GPS navigation most during deployment and re-entry near Florida, California and Texas. As a result, the Shuttle program may want to have an input to the determination process of placing these pockets or to change the criterion of optimization in selecting the satellite constellation.

Impact on Navigation Accuracy

The 18 SV constellation is expected to provide degraded performance relative to the original 24 SV network proposed. During certain time periods in isolated geographical regions, outages of GPS receivers are experienced. By outage is meant that the 3-D 1- σ range error exceeds 70

meters assuming a 1-D 1σ range error of 7 meters (P-code used) and 10 degree elevation mask angle. The nominal 1σ value is 16 meters. In the 3 orbit x 6 SV constellation studied by Aerospace Corporation, these outages last for about one hour 3 times a day in four major isolated areas on the oceans. Each area is a little over the size of CONUS.

If an altimeter is available with 1σ accuracy of 30 meters, the outage areas can be drastically reduced due to an improvement in measurement accuracy.

As an example, the following chart was shown:

Altitude Error	Accuracy	
	3D	2D
300M	335M	148M
30M	36M	21M

The altitude error is the 1σ error of an altimeter. With an error of 300M, the 3-dimensional position error is 335 meter and the 2-dimensional position is 148 meter for the worst case outage region. The accuracy is reduced significantly if a better altimeter is used.

Two other constellations are also studied: 18 orbit "rosette" (Philco Ford) and 6 orbit x 3 SV (STI). Similar outage patterns can be observed although the areas affected are much smaller and scattered. It appears that the 6 orbit x 3 SV constellation offers the best performance found so far. As a simple comparison the following chart was shown:

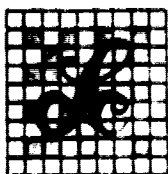
Percentage of Time Total Number of Satellites Visible

Constellation (Number of Orbital Planes)	5 Degree Elevation Angle Mask				10 Degree Elevation Angle Mask			
	Number of Satellites				Number of Satellites			
	4	5	6	7	4	5	6	7
3	100	92	72	40	98	?	?	?
18	100	77.6	77.8	30.8	99.9	86	44	7.6
6	100	99	78	28.7	100	90.4	41	5.9

Since 4 satellites are required for a normal position fix, the 6x3 configuration appears to achieve the best worst-case performance with a 10 degree elevation mask.

At this point, the ongoing studies for optimal constellation selection are driven by minimizing the percentage of outage areas on a world-wide scale. It appears that by modifying the orbits, these outage areas can be moved around.

Unclassified charts presented will be available to LinCom shortly and any pertinent data will be forward to JSC as soon as possible.



LinCom Corporation

INTEROFFICE MEMORANDUM
GPS-80-CMC-3

Date: November 4, 1980

From: C. M. Chie

cc: Bart Batson, Don Pusch,
Jack Johnson, Ann Sullivan

To: Jim Pawlowski

Subject: GPS Timing Structure and Typical Acquisition Sequence

Summary

This memo summarizes the timing structure of the received GPS signal and is simplified to highlight its impact on the normal acquisition procedure and time-to-first-fix (TTFF). In particular, the handover procedure from C/A-code to P-code is addressed.

1.0 GPS Signal Structure for Time Reference

A simplified GPS signal timing diagram is shown in Figure 1. All the information about the particular broadcasting satellite and the almanac of the GPS constellation are packaged in a 30 sec frame of data. The data frame is repeated every 30 secs starting from the end/start of the week (midnight Saturday night - Sunday morning). The data frame is divided into 5 subframes of 6 seconds each. In the beginning of each subframe there are a telemetry word (TLM) and a handover word (HOW) to help facilitate the transfer from C/A code to P-code. The TLM data slot contains a preamble and a telemetry message. The preamble is used to resolve the phase ambiguity involved with suppressed carrier tracking of the navigation message data which is NRZ coded. The HOW slot contains the truncated Z count which is the time (time of week) of the leading edge of the next subframe. The subframe ID is used to indicate the kind of information contained in the data block.

The 50 bps data is modulo 2 added (XOR) to the P-code (I carrier channel) and to the C/A code (Q carrier channel). The P-code is a composite code consisting of x_1 and x_2 . The period of x_1 is 15,345,000 chips long and spans 1.5 second. The all "1"'s epoch is lined up with the leading edge of the data subframe as well as the C/A code. The C/A code is 1023 chips long and spans 1 msec.

2.0 Normal Acquisition Sequence

In the normal acquisition sequence, the receiver first tracks the C/A code. Using the code epoch, it can determine the emitter's time to within an ambiguity of 1 msec. The receiver then proceeds to demodulate the data. Two pieces of information are sought at this point: the Z-count and the epoch of the next subframe leading edge. This information is used to set the local P-code generator so that it can be started at the same code phase as the incoming P-code at the upcoming subframe leading edge. This is possible since the x_1 epoch of the P-code, the C/A code, and the leading edge of the subframe all occur at the same instant. Note that if the receiver's clock is accurate to 1.5 secs, the Z-count can be generated internally by the receiver.

A detailed acquisition sequence is typically as follows:

I. C/A Code Loop Acquisition and Track

- a) Start C/A code search.
- b) C/A code loop pull in and track.

II. Data Demodulation

- c) AFC pull in.
- d) Costas loop pull in.
- e) Bit sync pull in and track.
- f) Ambiguity resolution and subframe sync (maximum 1 subframe = 6 sec after previous step).

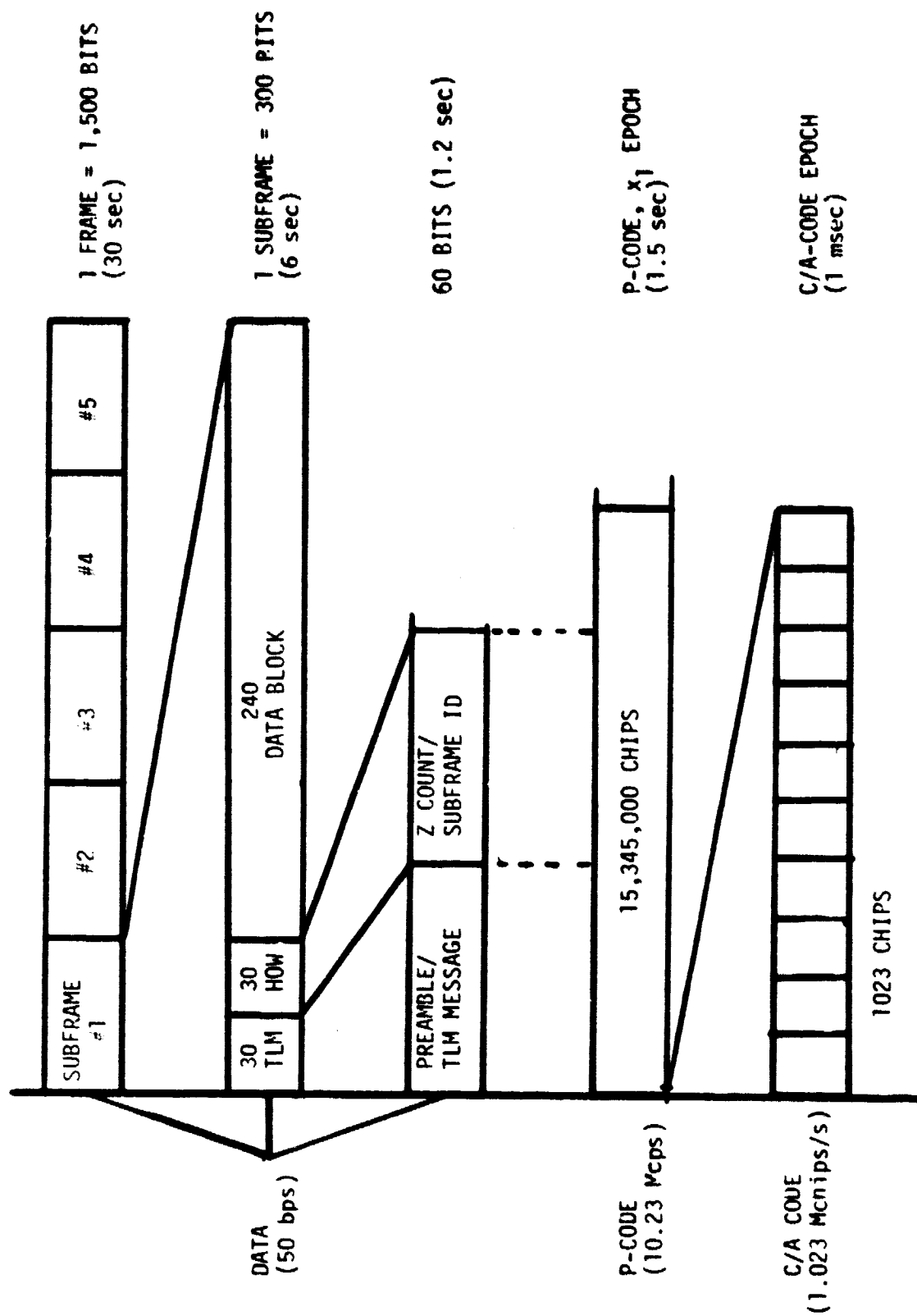
III. P-Code Handover

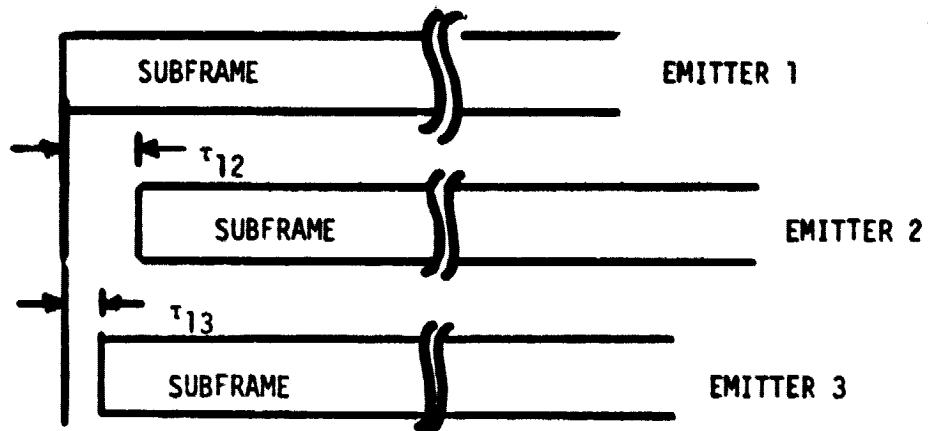
- g) Obtain Z count and align local P-code phase. Continue to demodulate data (need subframe 1, 2, and 3 to obtain clock error model, satellite ephemeris; need subframe 4 and 5 for message and almanac).
- h) P-code acquisition and track.
- i) Pseudo range and delta range measurement and initiates navigation software.

3.0 Notes

The range delay between a GPS emitter to a ground user and a second GPS emitter to the same user can be as high as 0.02 sec. The arrival epochs of the signals from three different emitters is depicted in Figure 2. Hence the HOW from one emitter cannot be used to pinpoint the 1.5 sec P-code epoch of another emitter which is lined up with the leading edge of the subframe of that particular emitter.

Figure 1. GPS Signal Timing Diagram.





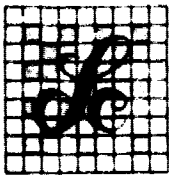
τ_{ij} = DIFFERENTIAL RANGE DELAY BETWEEN
EMITTER i AND EMITTER j TO THE
USER

Figure 2. Arriving Epochs from Different Emitters.

PROPOSED SPEC CHANGE

3.2.1.2.3.1 Normal Acquisition/State 1. In this state the R/PA shall acquire and track the NAVSTAR C/A signal aided by range and doppler estimates computed in the R/PA. When the handover word (HOW) is recovered from the 50 bps data stream the R/PA shall acquire and track the P signal. The R/PA shall track the carrier and demodulate data from the carrier. Pseudo and delta range measurements shall be made to full precision.

3.2.1.2.3.2 Direct Acquisition/State 2. In this state, the R/PA shall acquire the P signal without first acquiring its associated C/A signal. P code phase and frequency estimates for the acquisition shall be derived from almanac or current ephemeris data, present position and velocity estimates, and a precise input of Coordinated Universal Time (UTC). Direct P code acquisition shall be used to reacquire transmitters due to constellation revision and to improve anti-jamming margin when necessary.



LinCom Corporation

INTEROFFICE MEMORANDUM
GPS-81-CMC-1

Date: January 19, 1981

From: C. M. Chie

To: Dr. Jim Pawlowski

Subject: Magnavox PDR Review and NTC Highlights

cc: John MacLeod, Jack Johnson, William Teasdale, Ann Sullivan

SUMMARY

This memo serves to document a preliminary review of the Magnavox GPS Phase II PDR. Since the two-channel set is functionally similar to the Shuttle GPS R/PA baseline, some effort was spent on interpreting and understanding the TTF procedure for the two-channel set and the results are documented. In a forthcoming memo, we plan to compare the difference in TTF definitions used by Phase II set and the Shuttle GPS R/PA Spec.

During NTC, a paper was presented by Hewlett Packard (HP) for a low cost receiver. Judging from its schedule (approximately one year) and simple mechanization, it appears to be a viable candidate for the JSC GPS breadboard development program. Even though the receiver is rather unsophisticated, it does provide an opportunity to familiarize oneself with the operational aspects of using the GPS navigation signals.

Preliminary Review of the Magnavox GPS Phase II PDR

Based on the PDR notes (taken by Dr. Jim Pawlowski and Howard de Vezin), here are some comments of an overview nature:

- It appears that the design is geared towards operation in a high jamming environment.
- The concept of modularity/commonality is being stressed in order to tailor the set configuration to various host vehicle

requirements by simply assembling the receiver from common modules. This concept also permits major LSI development for common hardware components such as User Time Clock (UTC) and coders, etc.

- The significant improvements on the Phase II sets are on the operational aspects rather than functional aspects. For example, the following functions are highlighted:

- Automatic Fault Isolation (AFI)
- Alert and Status Display
- Self Test Capabilities

- In terms of receiver hardware realization, the five channel set is basically an X set; the one- and two-channel sets are based on the Z-set/Manpack concept.

- More attention is devoted to the interface requirements between the receiver and the host vehicle system for navigation aiding.

- It appears that the five-channel set can be adapted easily to meet the Shuttle GPS R/PA specifications in terms of dynamics and TTFF.

Dual Channel Acquisition Sequence

The normal acquisition sequence for a dual channel set in motion is depicted in Figure 1. The first half of the acquisition sequence is devoted to acquiring the C/A code. The second half operates on the P-code. After initialization, the first satellite signal is acquired using coordinated code search with the two available channels. Since the time uncertainty is specified to be 20S (1σ), the sequential code search is performed uniformly over the 1023 C/A code chips. Once the code signal is acquired in one channel (say channel 1 as in the figure), the receiver continues to perform:

- Code Loop Pull-In

- AFC to Center the Costas Loop
- Costas Loop Pull-In
- Bit Synchronization to Line Up the Bit Edge
- Resolving the Ambiguity Inherent in the Bit Sync from the TLM Word

The receiver then proceeds to demodulate the HOW and sets the user time using the HOW. (Notice that the GPS time can be determined from the HOW to within the range uncertainty between the user and the satellite which is in the order of 35 Km (1σ) or 120 C/A chips. Once the user time is set, the receiver can then change to a Gaussian 3σ search to acquire the remaining satellites. The Gaussian search is much more efficient time-wise and amount to substantial TTF savings.) Channel 1 then continues to take pseudo range and delta range measurements. It then filters these measurements and prepositions the VCO for the code signal from the third satellite.

Once the first channel verified the presence of the code signal, the receiver on the other channel (Channel 2) starts the uniform search for the second satellite. If the first channel can read the HOW and set the user time before the acquisition of the second satellite in Channel 2, the second channel will switch to the Gaussian search mode. The receivers continue to acquire and measure the rest of the signals as indicated in the figure. Before switching to tracking the P-code, the set reacquires the satellite signals again to compensate for any untracked motions between the user and the satellites during the gap between the channel sequence. After the C/A to P code handover is completed, the set proceeds to calibrate out the differential hardware delays between the two channels (including L_1 and L_2 frequencies). This

can be done by tracking the same satellite signal using both channels. The set then proceeds to demodulate ephemerides data from the satellite signals. First of all, it must wait for the frame sync and starts collecting data from the first two satellites during subframes 1, 2, 3 (18 sec). During subframes 4, 5, the set reacquires the remaining satellite signals and collects data when the next frame sync comes up. The set then makes the ionospheric measurement and starts the sequential tracking (or dwell). After one cycle of the sequential track, the first fix is available.

The total Time-to-First-Fix TTF is 203.1 sec for a set in motion. Notice that 60 sec is devoted to ephemerides collection, a maximum of 30 sec can be wasted for waiting for frame sync (FS), and there is a maximum of 6 sec to wait for the TLM word to resolve the bit sync ambiguity for each signal.

Low Cost GPS Receiver by HP

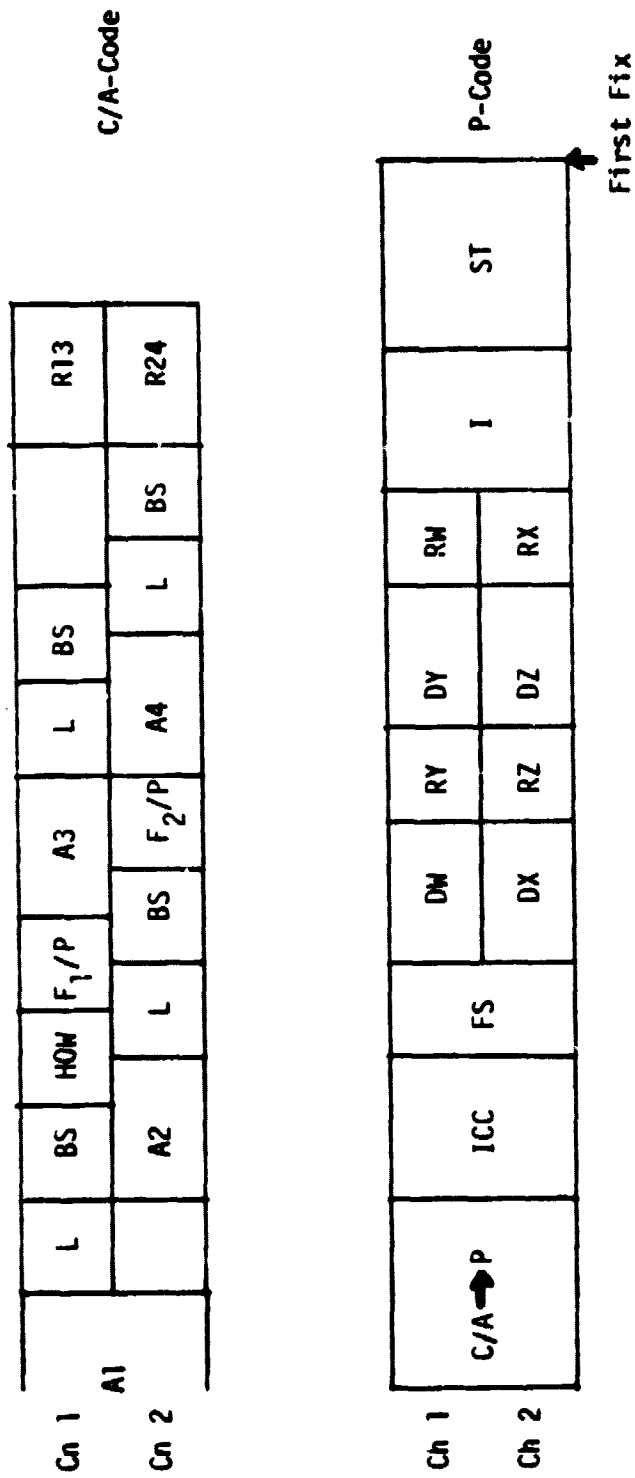
The low cost GPS receiver built and tested by HP was designed to meet the requirements of land navigation with limited mobility (i.e., stationary or up to 60 mph). It was initiated in 1977 and built and tested successfully in 1978. Apparently, two engineers were involved (level of support?). The HP receiver is a sequential one-channel set using C/A code on the L_1 carrier. The test results showed an accuracy of 20 meters. A Z-80 microcomputer is used for receiver control while the navigation computations are performed on an HP9825 desktop calculator (see Fig. 2). The navigation solution for the position and clock bias is computed iteratively. No attempt is made to smooth out consecutively fixes with Kalman filtering. Hence, the computations involved are basically for solving a four-dimensional nonlinear

equation.

Reference

K. P. Yiu, et al., "Land Navigation with a Low Cost GPS Receiver," NTC,
December 1980, Houston, Texas, pp. 55.3.1-55.3.7.

Figure 1. Dual Channel Acquisition Sequences for Moving GPS Receivers.



LEGEND:

- | | |
|--------------------------------|---|
| F/P - Filtering & Preposition | DW - Ephemeris Data from Satellite #1 (18s) |
| A1 - Acquire Satellite #1 | RW - Reacquire Satellite #1 (12s) |
| L - Loop Pull-in | I - Ionospheric Measurement |
| BS - Bit Sync | ST - Sequential Track |
| HOW - Read Hand Over Word | |
| R1 - Reacquire Satellite #1 | |
| ICC - Interchannel Calibration | |
| FS - Frame Sync (30 sec) | |

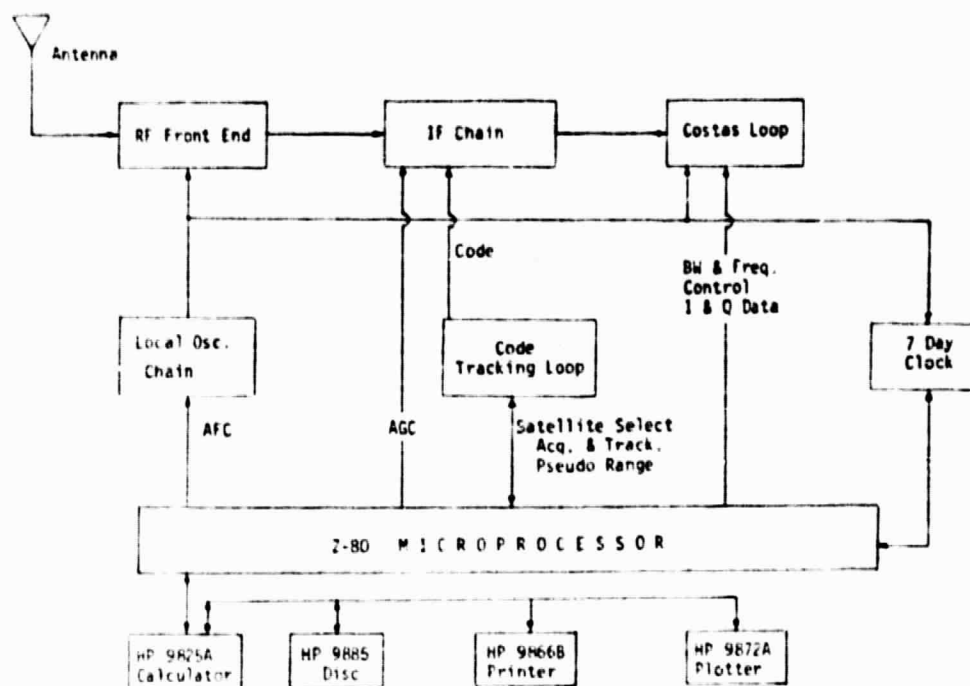


Figure 2. Block Diagram of the GPS Receiver.



LinCom Corporation

INTEROFFICE MEMORANDUM

GPS-81-CMC-2

Date: February 17, 1981

From: C. M. Chie

To: Dr. Jim Pawlowski

Subject: Bit Synchronization and Message Demodulation for GPS Signal

cc: John MacLeod, Jack Johnson, William Teasdale, Jack Seyl, Don Pusch, D. Poland

Summary

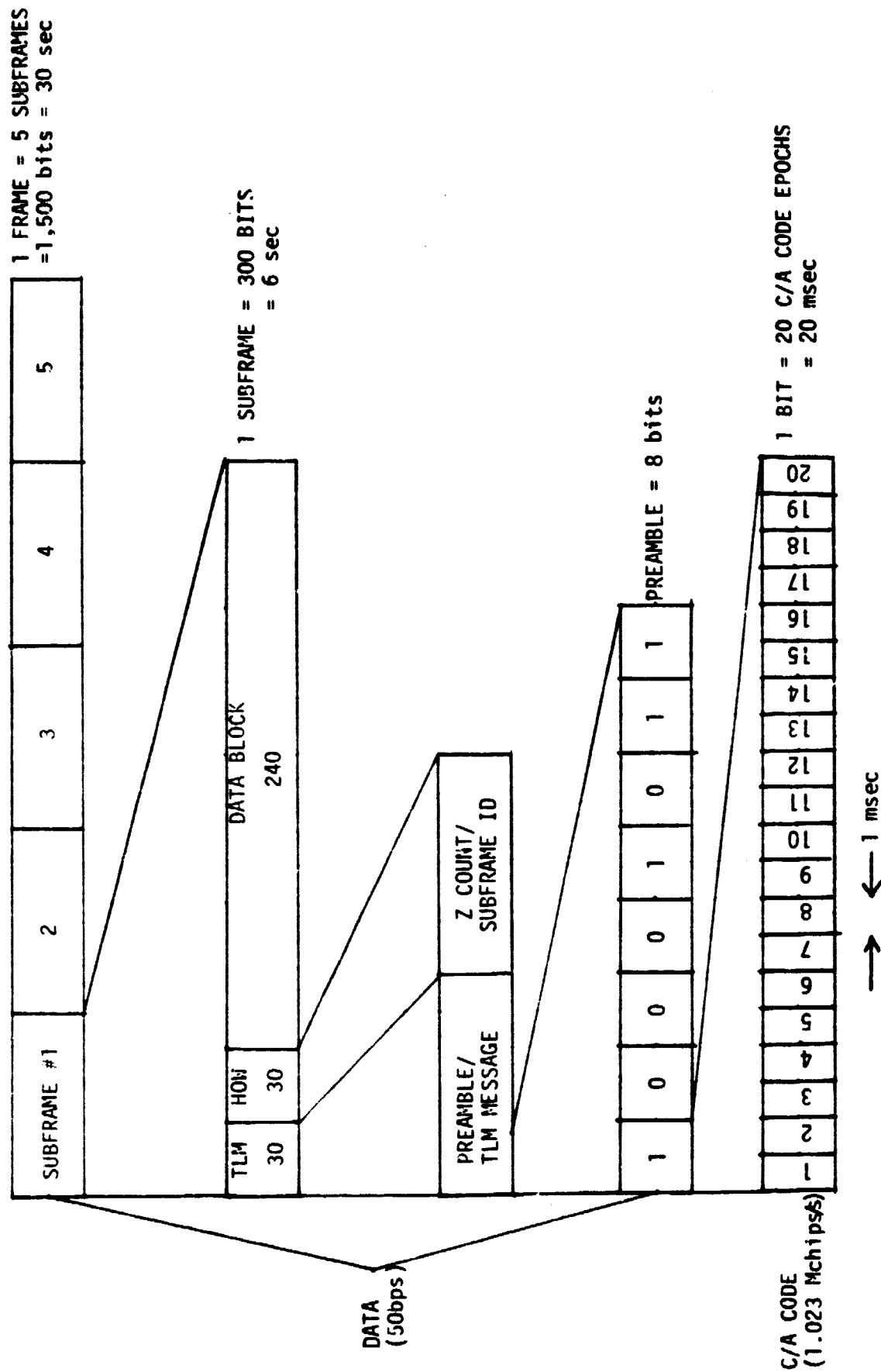
A hardware and a software method for obtaining bit and subframe synchronization are described in this memo. It appears that the hardware method is more appropriate for the GPS breadboard development program.

GPS Message Timing Structure

Figure 1 shows the timing structure of the received GPS message. The message is structured to facilitate data demodulation. The important feature is that the C/A code epochs (and P-code epochs) are coherent with the data bit boundary and each data bit is equal to 20 complete C/A code periods. Each subframe starts with a preamble word (10001011) whose purpose is two-fold: (a) to signal the start of a subframe and (b) to provide a means to check the polarity of the demodulated data.

In this memo, we assume the code loop is in lock, i.e., the C/A code epochs are available. Before we proceed to demodulate the navigation ^{data}, we must resolve the following ambiguity conditions:

Figure 1. GPS Message Timing Structure.



- (a) code epoch ambiguity - determine which one of the 20 code epochs is coherent with the bit clock.
- (b) data bit inversion ambiguity - determine whether the demodulated bit has been inverted.
- (c) subframe ambiguity - determine which bit is the start of a subframe.

The first ambiguity condition is resolved by means of a bit sync circuit (or procedure). The second and third ambiguity conditions are resolved by the preamble word.

Typical Bit and Subframe Synchronization - Hardware Approach

A hardware approach for bit and subframe synchronization procedure for resolving the ambiguity conditions described in the last paragraph is exemplified by the techniques used in the Stanford Telecommunications Inc. (STI) Geodetic System Receiver. Figure 2 shows the circuit for C/A bit sync and data detection and Figure 3 shows the subframe sync procedure.

The bit sync circuit operates by checking for data transitions around each epoch (20 possible epochs per bit). There are 20 accumulators keeping track of the transitions scored by a particular epoch. After one of the accumulators fills up to $2^6 = 64$ counts, the associated epoch is declared to be the data bit boundary and the data clock is set accordingly. The data clock is used to provide the timing for the 20 millisecond integrate and dump circuit for the data detector.

In order to simplify hardware, the possible data transition is determined by looking at portions of 1/20 bit as shown. The transition detector shown in Figure 2 can be a simple comparator. Notice that since only 1/20 of a bit is integrated, the signal-to-noise ratio

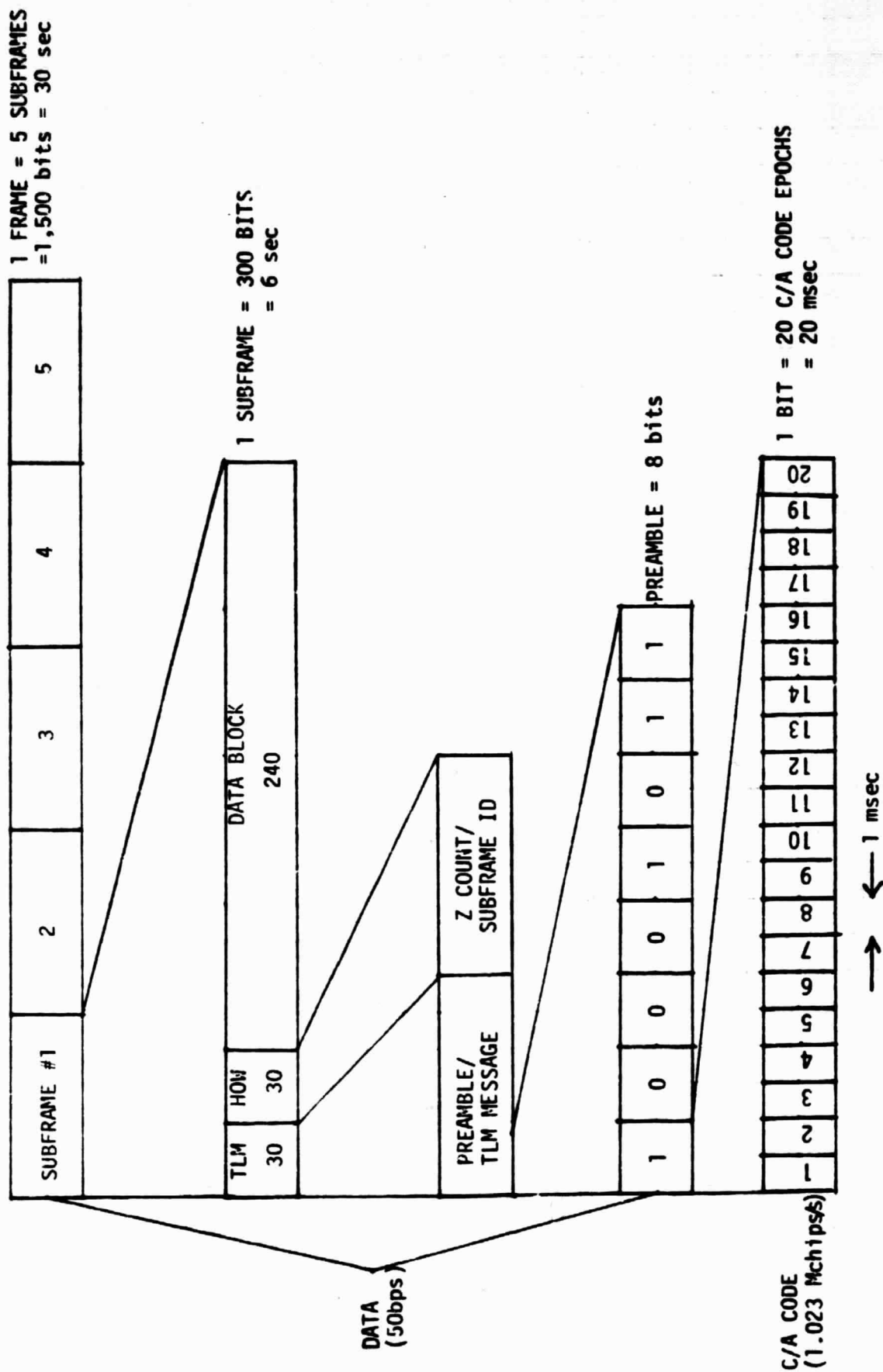
degrades by 13 dB. To compensate for this degradation, the accumulators are used. The signal-to-noise ratio improvement is proportional to the number of transitions observed before declaring "lock". Further analysis is necessary to determine the appropriate accumulator size for a particular operational requirement.

In Figure 3, the navigation data from the data detector output of the previous figure is resolved by matching the data stream with the preamble pattern. Once a match is found the data is inverted accordingly and subframe sync is declared. The HOW is then demodulated and used to set the local receiver time.

Typical Bit and Subframe Synchronization - Software Approach

A software approach for bit and subframe sync is typified by the Magnavox X-set. The principle of operation is very similar to the hardware approach. Excerpts enclosed describing the procedure are from an Air Force Report SAMS0 TR77-102 Vol I entitled A Functional Description of the Navstar GPS Receiver Model X. Note that the software approach is appropriate here because the X-set is a digital receiver and the 1 msec, 1/20 bit samples are readily available from the carrier channel output.

Figure 1. GPS Message Timing Structure.



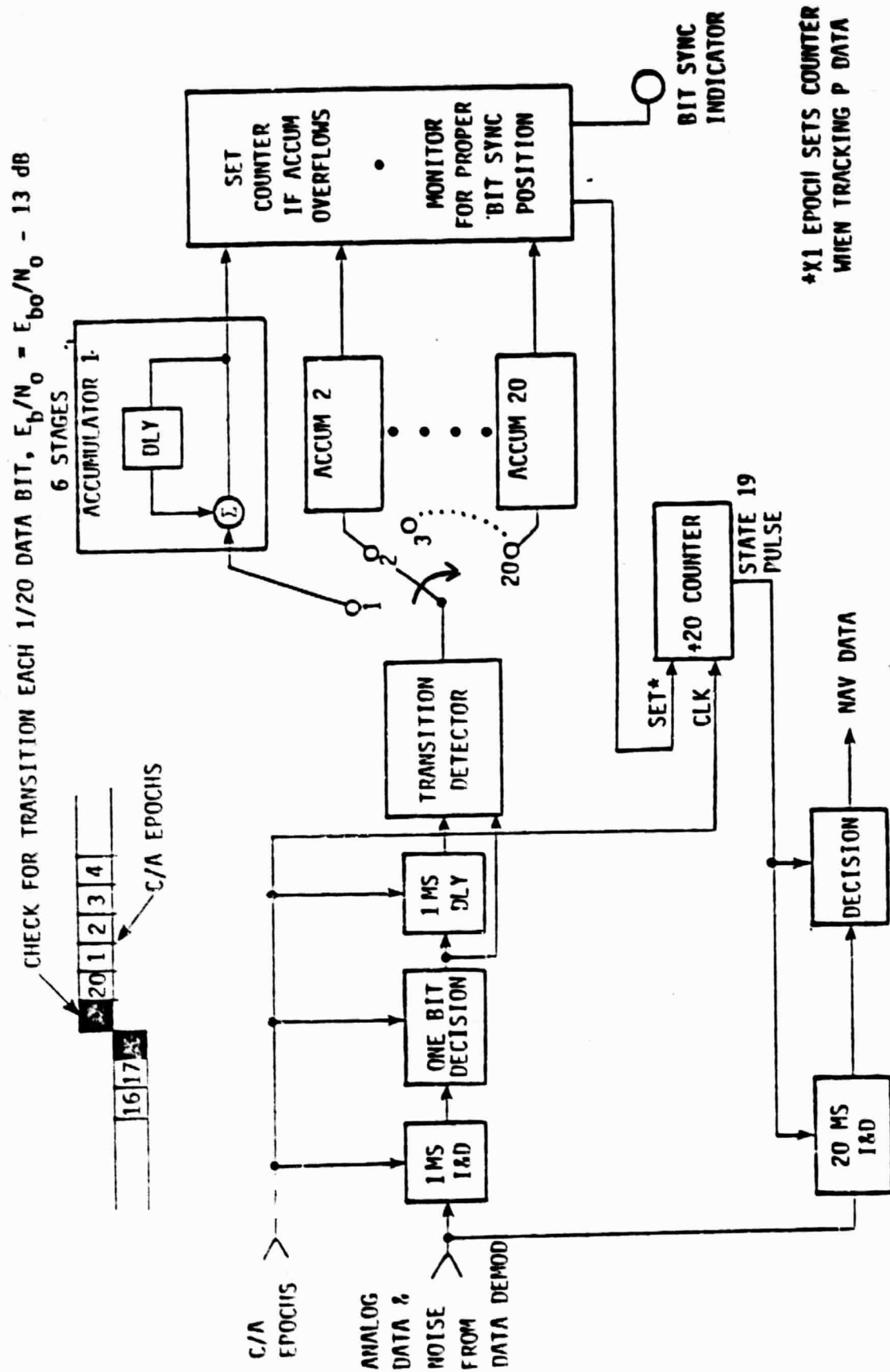


Fig. 2. C/A BIT SYNC RESOLUTION & NAV DATA DETECTION

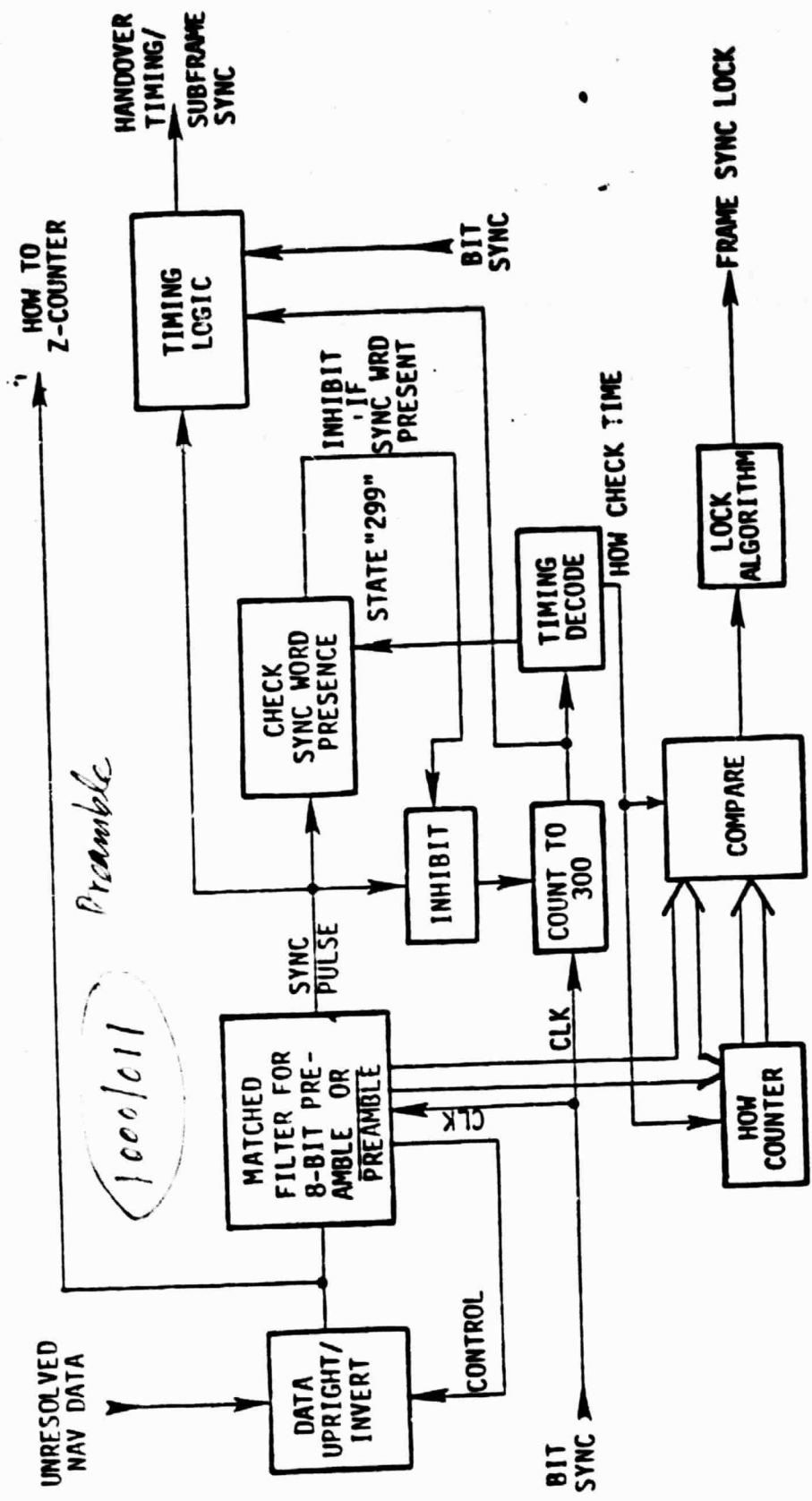


Fig. 3. SUBFRAME SYNC AND HOW TIMING BLOCK DIAGRAM

PREAMBLE ONLY
8 BITS

- MAKE USE OF 1) PERIODICITY OF SUBFRAME SYNC PREAMBLE
2) INCREMENTING HOW WORD FOLLOWS PREAMBLE AT
SPECIFIC DISTANCE

AIR FORCE REPORT
SAMSO TR 77-120
VOLUME I

R-981
A FUNCTIONAL DESCRIPTION OF THE
NAVSTAR GPS RECEIVER MODEL X
FINAL REPORT FOR
SAMSO CONTRACT F04701-75-C-0212
VOLUME I
by
William M. Stonestreet
26 April 1976
Revised February 1977



The Charles Stark Draper Laboratory, Inc.
Cambridge, Massachusetts 02139

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X-set

Section 11. Data-Bit Synchronization

After Costas lock has been achieved the receiver synchronizes the user-time clock to the incoming data bits. The NDLL is tracking the C/A code which is synchronized to the data-bit transitions. However the C/A code repeats every one millisecond whereas data-bit transitions occur less frequently, every twenty milliseconds. Thus using only information from the NDLL, the receiver can accurately locate the data-bit transitions within a one-millisecond interval but is unable to determine which of twenty possible one-millisecond intervals in which the data-bit transition occurs. A histogram of the sum of the sign reversals of the inphase samples of the received signal in each of twenty one-millisecond time intervals is used to resolve this ambiguity. One second of inphase samples (or equivalently fifty data bits) is used to form the histogram. The sum of the sign reversals in the one-millisecond interval which coincides with the data-bit transition must be larger than the sum in any other one-millisecond interval by at least ten sign reversals. When this is true, data-bit synchronization is declared. When data-bit synchronization has been declared the user-time clock is appropriately advanced or delayed to coincide with the data-bit transition. Then the integrate-and-dump interval is set to four milliseconds. The receiver then enters the data-frame synchronization mode.

If at any time during the data-bit synchronization process Costas lock is lost, the procedure starts over. This prevents cycle skipping from being interpreted as data-bit transitions.

A flow diagram of the data-bit synchronization process is shown in Figure 24.

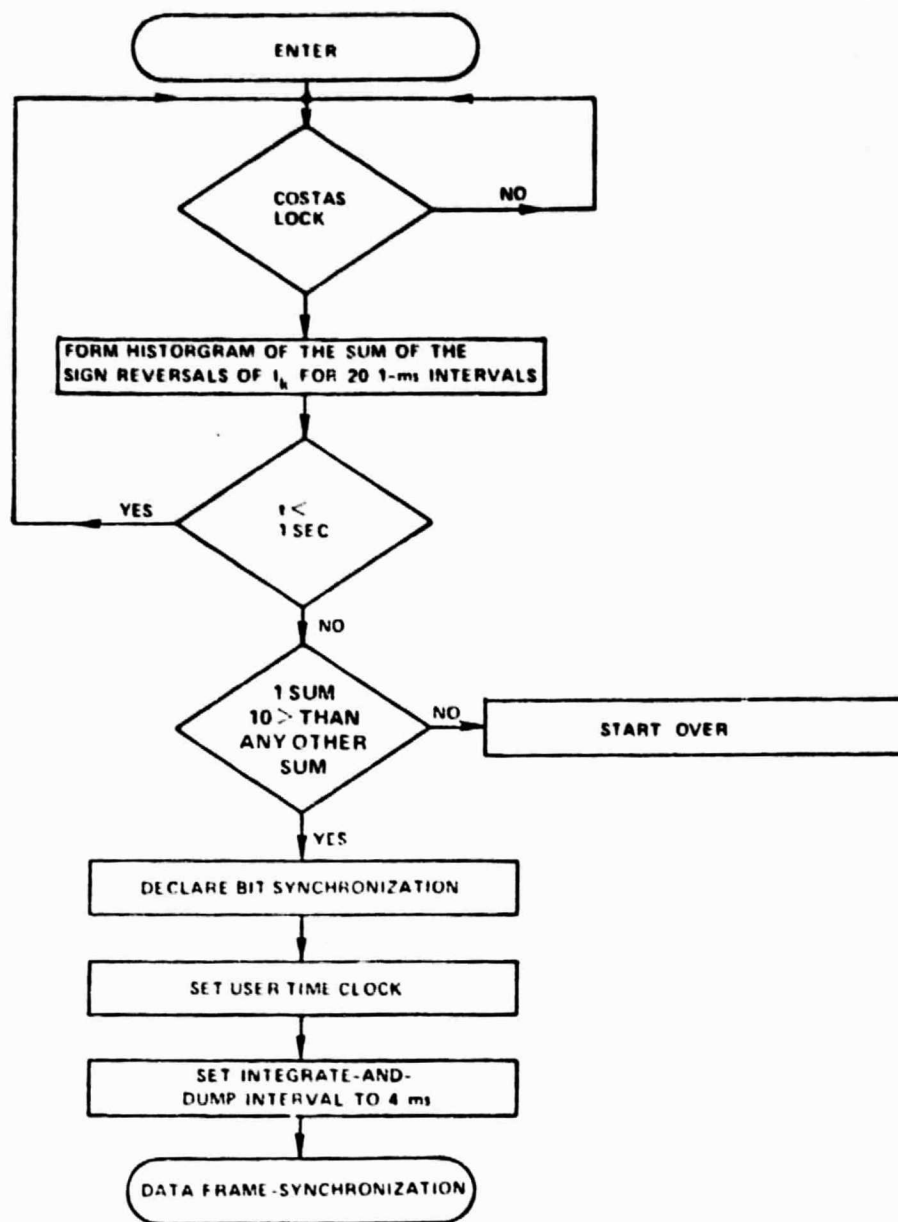


Figure 24. X-Set Data-Bit Synchronization Procedure
From References [1,3]

Section 12. Data-Frame Synchronization

After data-bit synchronization the receiver must be synchronized to the data frame being transmitted. A flow diagram of the data-frame synchronization process is shown in Figure 25. The process controller demodulates the data bits and compares them with the synchronization bits (preamble) of the telemetry word and their logical inverse. (The telemetry word is uniformly distributed in the data frame and occurs every six seconds). When the preamble or its logical inverse is detected the remaining bits in the telemetry word are demodulated and a parity check is performed. If a parity error is detected, the process starts over. If not, the handover word is demodulated and a parity check is made on it. As before, if a parity error is detected the process restarts. If not, the current subframe is identified, the pseudo-range and user-time clock are set, and tentative data-frame synchronization is declared. The remaining data until the next handover word is demodulated, and a parity check is performed. If the Z-count (system time) of the next handover word differs from the previous Z-count by more than one, data-frame synchronization is cancelled and the procedure is restarted. If the difference is exactly one, data-bit and data-frame synchronization are performed for the other channels that are Costas locked. Then the pseudo-ranges of the channels are compared. If any of them differ by more than 21 ms, data-frame synchronization is cancelled and the process is restarted. However, if the differences are less than 21 ms, data-frame synchronization is declared.

The comparison of pseudo-ranges is a reasonability test. Twenty-one milliseconds of the C/A code corresponds to approximately 4000 miles. The maximum pseudo-range difference will exist when one of the satellites is directly overhead and one near the horizon. There is approximately 4000 miles pseudo-range difference between a satellite directly overhead and one 15° above the horizon. Normally satellites with elevation angles lower than 15° above the horizon will not be used for navigation. Thus, if the pseudo-range difference is greater than 4000 miles the user-time clock has probably been incorrectly set and the data-frame synchronization process (which sets the user-time clock) is repeated.

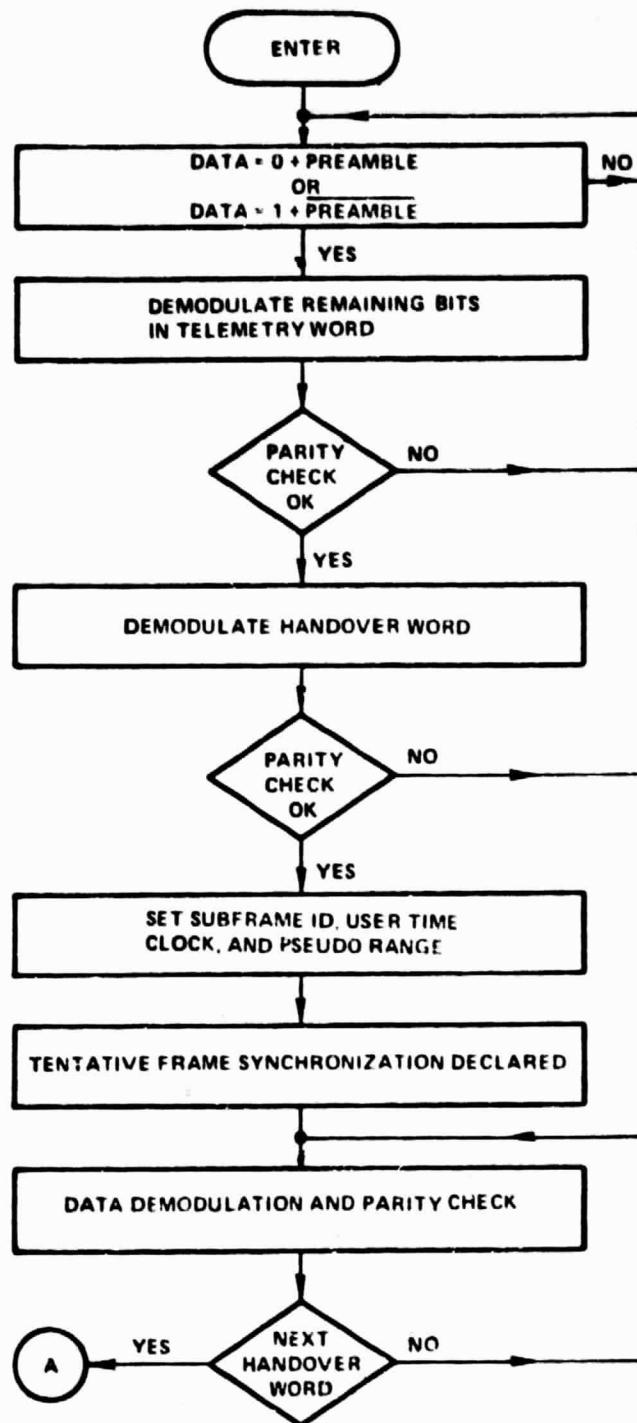


Figure 25. X-Set Data Frame Synchronization
From Reference [3]

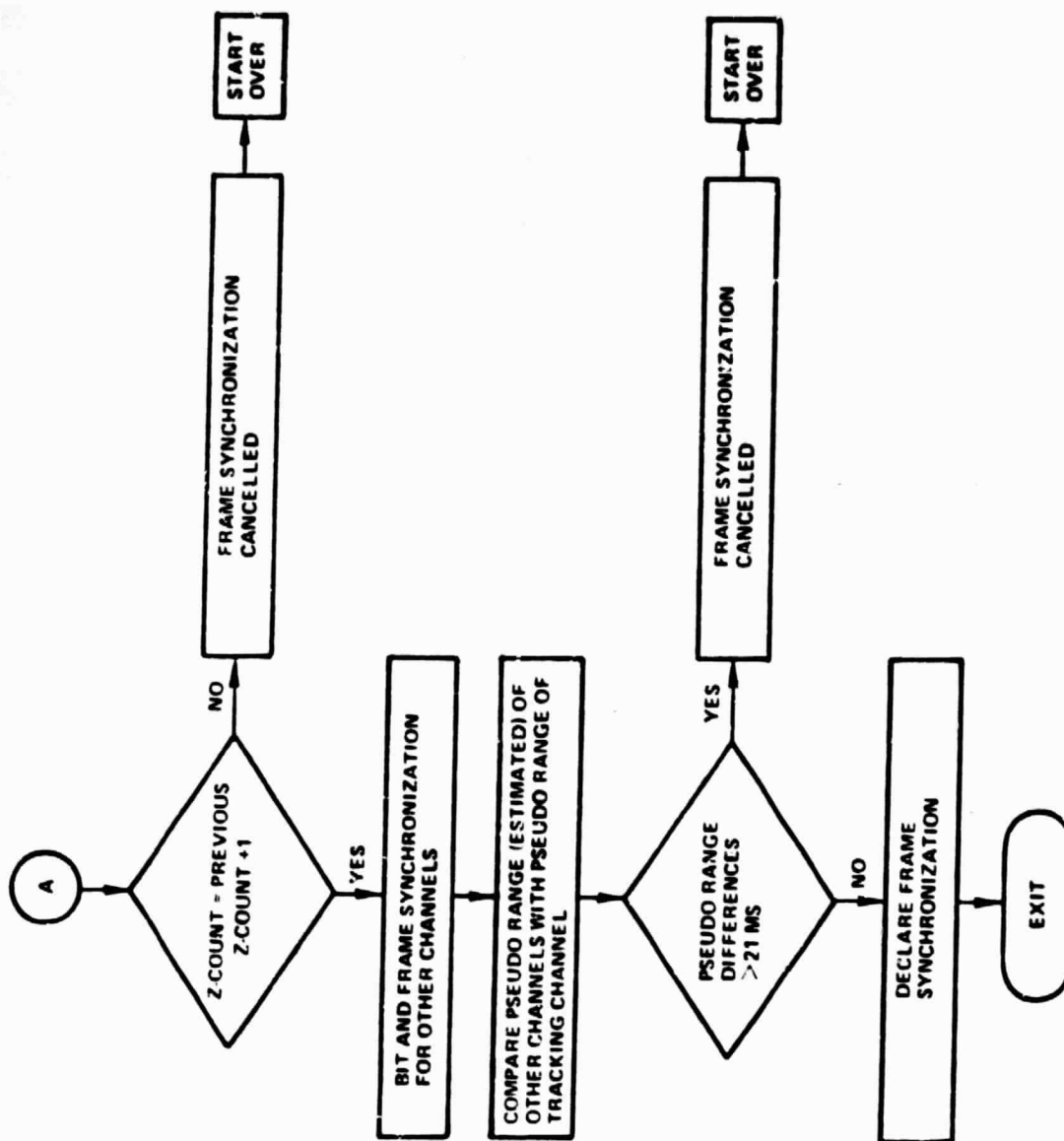


Figure 25. X-Set Data Frame Synchronization (Continued)
From Reference [3]



LinCom Corporation

INTEROFFICE MEMORANDUM

GPS-81-CMC-3

Date: April 8, 1981

From: C. M. Chie

To: Dr. Jim Pawlowski

Subject: Considerations for Testing GPS Receivers Using a Single GPS Signal Simulator

cc: John MacLeod, Jack Johnson

Summary

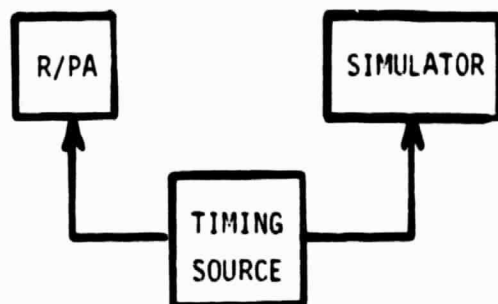
The attached package of notes summarizes a preliminary investigation of the problems and options associated with testing the GPS receiver. In particular, the emphasis is on testing the GPS receiver when only one simulated emitter signal (out of a total of a complete set of four) is available. The first part of the package is a general description of the ideal test configuration and the basic system and subsystem tests required to determine receiver performance.

The implications of testing with a nonideal configuration, for example, with 1 satellite simulator, are then considered. Special attention is devoted to the 2-channel sequential set (present JSC baseline). Supplementary tests that can be performed independent of the simulator signals are also highlighted.

Additional Comments

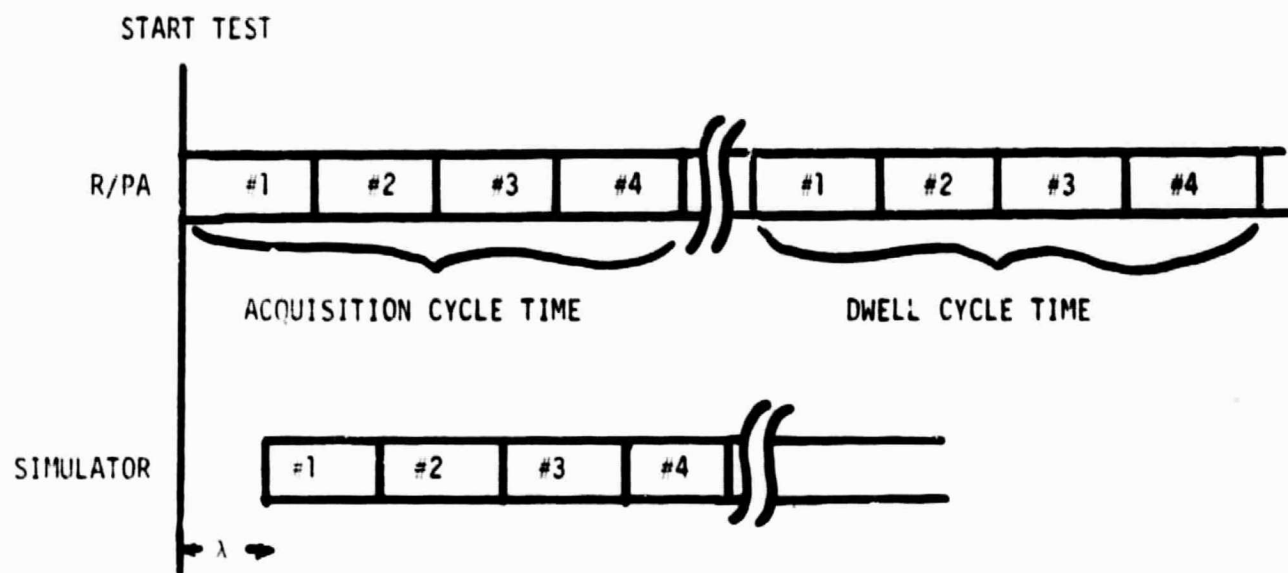
The material was discussed over the phone with Dr. Jim Pawlowski on March 25, 1981. At that time several additional comments were made. The following is a summary. (Items 1 and 2 were discussed while going through ways to fool a one channel sequential set.)

- (1) In order to reduce the interface requirement of the R/PA with the outside world, it was suggested that the simulator be programmed to switch emitter signals independently at approximately the same time as the R/PA. Figure 1 demonstrates the potential difficulties.
- (2) Another scheme for synchronizing the R/PA and the simulator is through an external timing source, i.e.,



This requires the R/PA to accept external sequencing controls.

- (3) The R/PA design may want to incorporate some sort of "data" testing capabilities (i.e., provide test access points to the right of the dashed line in the R/PA functional block diagram in the package.) The advantage is that the digital/computational/control portion of the R/PA can be checked out more rapidly and independent of the RF section.
- (4) Consider R/PA procedures for entering into, staying in and recovering from a blackout.
- (5) Consider R/PA procedures when less than 4 emitters are visible.
- (6) Provide capability for the R/PA to track a single satellite continuously for testing purpose.
- (7) Consider R/PA test access points and externally controllable functions based on selected testing philosophy in the next round of spec revision.



- ACQUISITION CYCLE TIME CAN BE DIFFERENT FROM DWELL CYCLE TIME; TIME FROM START TO DWELL MAY BE RANDOM AND HENCE CANNOT BE PREDICTED FOR THE SIMULATOR
- SYNCHRONIZATION ERROR REDUCES CORRECTLY RECEIVED SIGNAL DURATION
- RELATIVE DRIFTS

Figure 1. Timing Diagram for R/PA and Simulator.

LinCom

CONSIDERATIONS FOR TESTING GPS
RECEIVER USING ONE SIMULATOR

PREPARED FOR
NASA JOHNSON SPACE CENTER
HOUSTON, TX 77058
CONTRACT NO. NAS9-16097

PREPARED BY
C. M. CHIE
LINCOM CORPORATION
P.O. BOX 2793D
PASADENA, CA 91105

MARCH 1981

LinCom

GPS RECEIVER TESTING CONSIDERATIONS

3 TYPES OF RECEIVERS

- 1 CHANNEL (SEQUENTIAL)
- 2 CHANNEL (SEQUENTIAL)
- 5 CHANNELS (PARALLEL)

● SATELLITE SIMULATOR AVAILABILITY

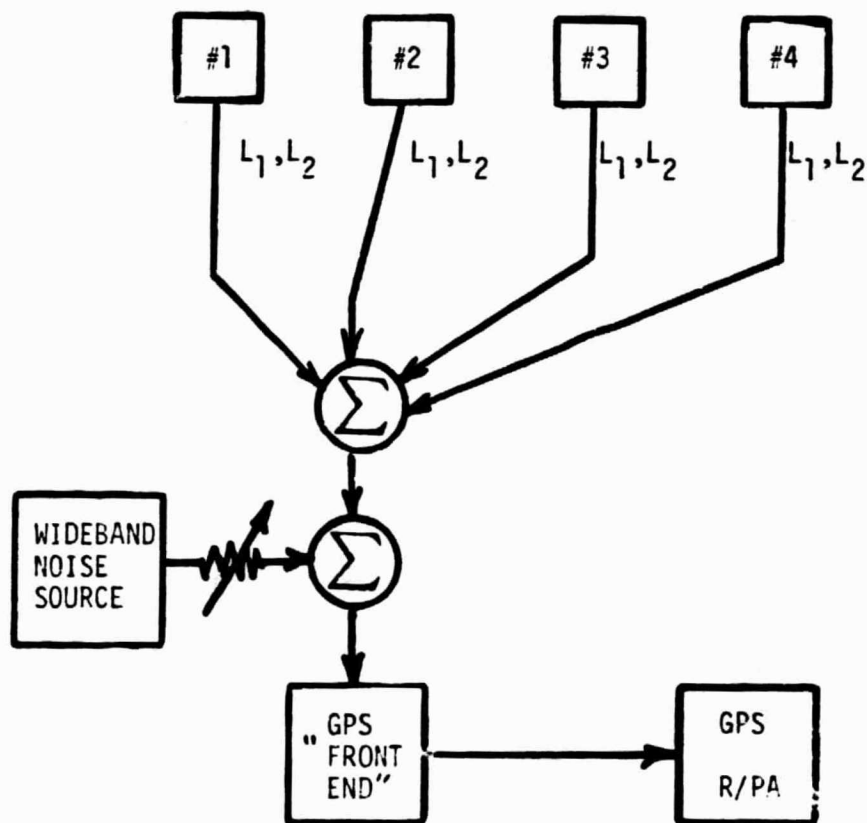
- 4 SIMULATORS
- 1 SIMULATOR

● SIMULATOR/RECEIVER INTERFACE REQUIREMENTS

- DEPENDS ON ABOVE
- IMPACT ON RECEIVER DESIGN W.R.T. TEST ACCESS POINTS AND RECEIVER CONTROL
- "FIELD" TESTS
 - TESTS PERFORMED WITH ACTUAL SATELLITE SIGNALS

IDEAL TEST CONFIGURATION

SIMULATOR



SUBSYSTEM AND SYSTEM TESTS REQUIRED

FOR COMPLETE TESTING OF R/PA

SYSTEM LEVEL TESTS

- SATELLITE SELECTION
- TIME-TO-FIRST-FIX
- R/PA ACCURACY
 - PSEUDO-RANGE
 - RANGE-RATE
- NAVIGATION ACCURACY

SUBSYSTEM LEVEL TESTS

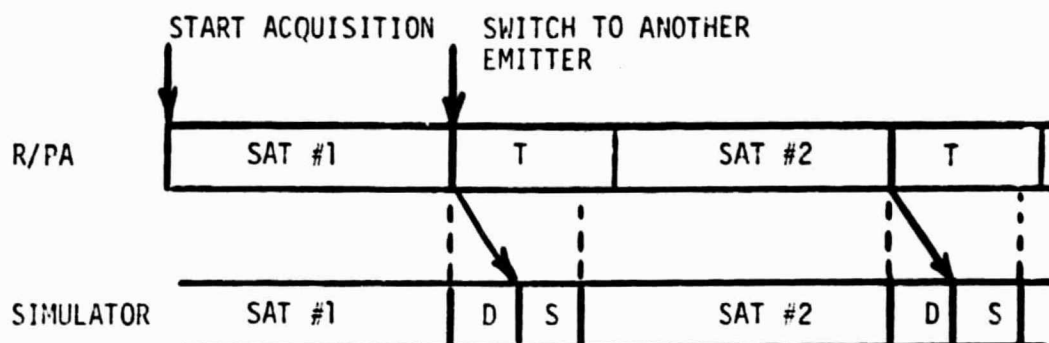
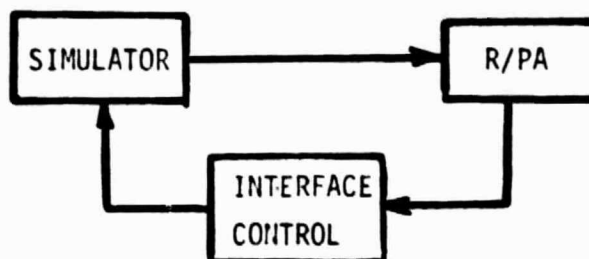
- RECEIVER HARDWARE
 - CODE LOOP
 - ACQUISITION
 - TRACKING
 - CARRIER LOOP
 - ACQUISITION
 - TRACKING
 - BIT SYNCHRONIZER
 - FRAME SYNCHRONIZER
 - CODERS
 - USER TIME CLOCK
- RECEIVER CONTROL
 - ACQUISITION
 - CHANNEL SEQUENCING
 - FREQUENCY PREPOSITIONING
 - CODE PREPOSITIONING
 - CONSTELLATION REVISION
- NAVIGATION SOFTWARE
 - POSITION FIXES
 - TIME FIXES

IMPACTS ON TESTING CAPABILITIES

WITH ONE SIMULATOR AVAILABLE

- ONE CHANNEL SEQUENTIAL
 - FULL-SCALE TESTING POSSIBLE PROVIDED
INTERFACE REQUIREMENTS ARE MET
- TWO-CHANNEL SEQUENTIAL
 - PARTIAL TESTING ONLY
 - FULL-SCALE TESTING POSSIBLE WITH 2 SIMULATORS
- 5 CHANNEL PARALLEL
 - PARTIAL TESTING ONLY

SEQUENTIAL ONE-CHANNEL SET INTERFACE REQUIREMENTS



- T IS THE TRANSITION TIME REQUIRED TO PREPOSITION THE FREQUENCY AND CODE FOR A SECOND EMITTER
- S IS THE SWITCHING TIME REQUIRED TO CHANGE FROM ONE EMITTER SIGNAL TO ANOTHER
- D IS THE TIME DELAY REQUIRED TO RELAY THE SWITCHING OF R/PA TO SIMULATOR
- IF $D+S < T$, THE R/PA IS COMPLETELY FOOLED BY ONE SIMULATOR

SEQUENTIAL TWO CHANNEL SET

- CANNOT FOOL R/PA COMPLETELY
- TYPICAL SEQUENCING

CHANNEL 1	SAT #1	SAT #3
CHANNEL 2	SAT #2	SAT #4

- SIMULATOR CANNOT GENERATE 2 CHANNELS SIMULTANEOUSLY
- PARTIAL TESTING POSSIBLE (ESPECIALLY HARDWARE)
- SUPPLEMENTARY TESTS REQUIRED

OPTION #1

- FORCES 2 CHANNEL R/PA TO WORK AS TWO SEQUENTIAL 1 CHANNEL RECEIVER OPERATING ON L_1 AND L_2

CH 1 (L_1)

EMITTER #1	#2	#3	#4	#1
------------	----	----	----	----

CH 2 (L_2)

EMITTER #1	#2	#3	#4	#1
------------	----	----	----	----

- COMPLETE TESTING POSSIBLE

OPTION #2

- PROVIDE CONTROL CAPABILITY TO R/PA SO IT CAN TRACK SAME
EMITTER MORE THAN ONCE

CH 1	SAT #1	SAT #2	SAT #1	SAT #2
CH 2	#1	#2	#1	#2

OR

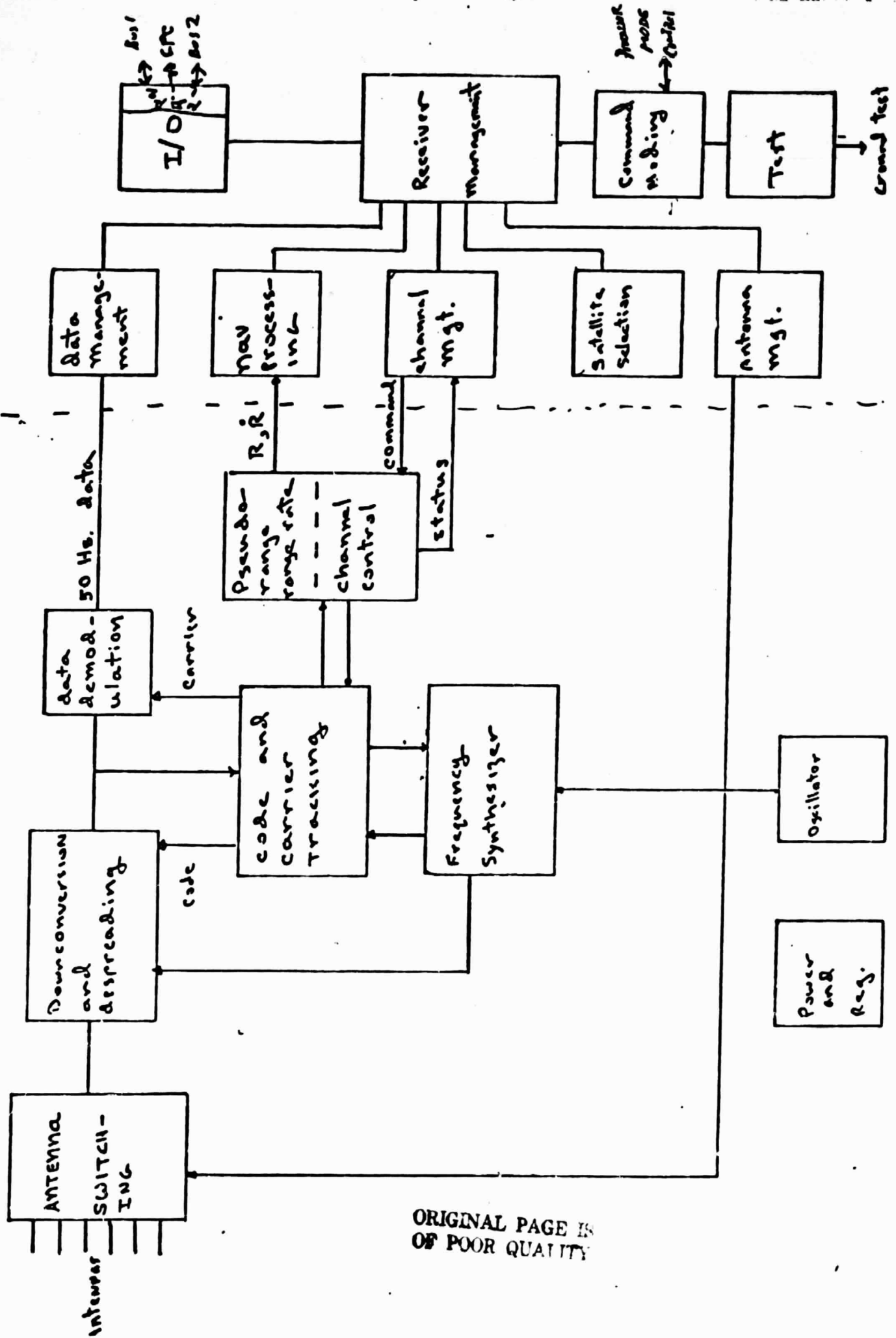
CH 1	#1	1	1	1
CH 2	1	1	1	1

- IMPACTS:
 - POOR SYSTEM LEVEL TESTING
 - POOR GDOP
 - RECEIVER HARDWARE TEST OK
 - RECEIVER CONTROL OK EXCEPT FOR CONSTELLATION REVISION
 - NAVIGATION SOFTWARE
 - POOR GDOP

SUPPLEMENTARY TESTS

- ADDITIONAL TESTS NEEDED (WITHOUT USING SIMULATOR)
- COMPUTER PROCESSING PORTION OF R/PA CAN BE TESTED BY COMPUTER SIMULATION (SEE FIGURE)
- OVERALL SYSTEM LEVEL TEST MUST BE VERIFIED WITH ACTUAL GPS SIGNALS

Replacement for Figure 1.



R/P/A Functional Block Diagram

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5 CHANNEL SET

- PROBLEM VERY SIMILAR TO 2-CHANNEL SET

LinCom

PROGRESS REPORT

SHUTTLE GLOBAL POSITIONING SYSTEM (GPS)
IMPLEMENTATION STUDY

PREPARED FOR

NASA LYNDON B. JOHNSON SPACE CENTER
HOUSTON, TX 77058

TECHNICAL MONITOR: DR. JIM PAWLOWSKI, CODE EE8

CONTRACT NO. NAS9-16097

PREPARED BY

LINCOM CORPORATION
P.O. BOX 2793D
PASADENA, CA 91105

APRIL 1981

Summary

In LinCom's last report [1] we described a method of obtaining bit and subframe synchronization. In this report we present the analysis and the performance of the bit synchronization technique presented to portray relationships between the SNR and the probability of correct detection of the bit synchronization circuit along with the average wait time for each decision.

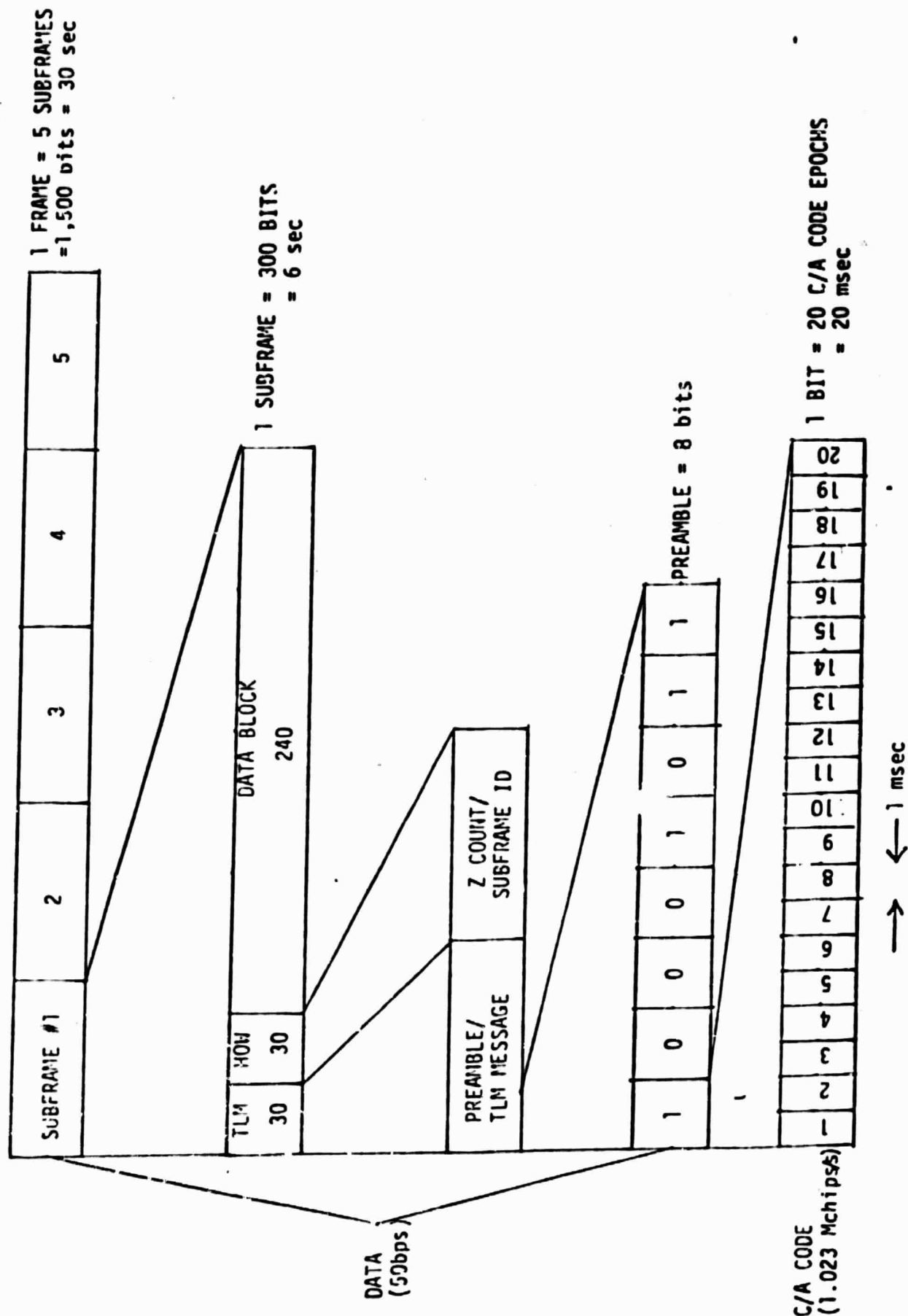
The results are presented for the relevant CNR range of $29 \leq C/N_0 \leq 36$ dB-Hz which when converted to the bit signal to noise ratio SNR becomes $12 \leq \text{SNR} \leq 19$ dB. From the curves presented in this report one can say that for a probability of correct detector of 0.99 and an SNR of 10.2 dB it would be necessary to have the shift register length of at least 5 and the average waiting time to make a decision would be about 1.2 seconds.

1. GPS Signal Structure and Bit Synch Circuit

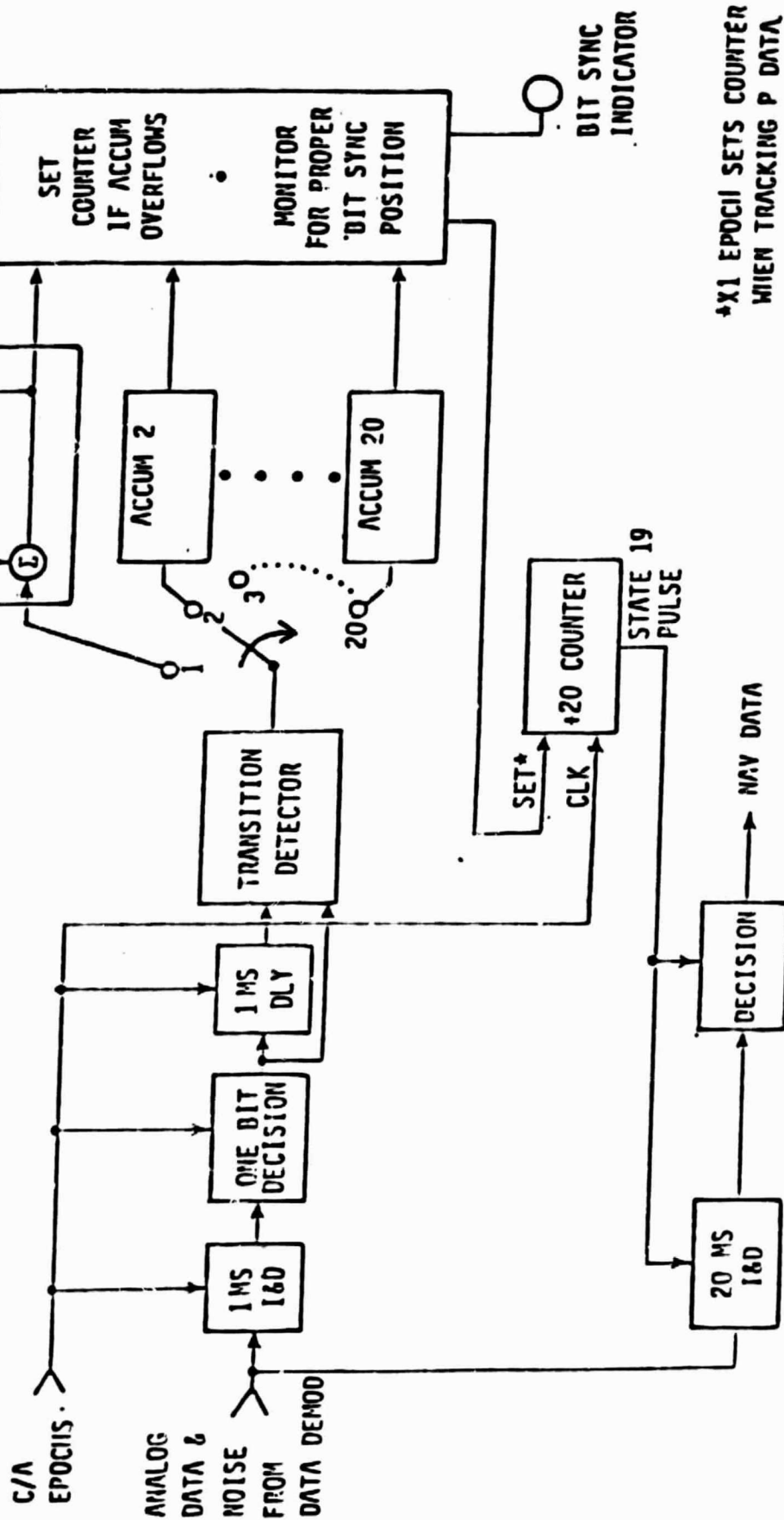
The incoming GPS signal at any receiver has the C/A (clear acquisition code), the P (precision timing) code and the data message. One important thing to notice here that the C/A code epochs (1000 epochs per second), P code epochs (1 epoch in every 1.5 seconds) are coherent with data bit boundary, (50 boundaries per second). Thus each data bit contains exactly 20 C/A epochs, i.e. within every count of 20 of the C/A epochs, one and only one C/A epoch is coincident with the data bit boundary. In this report analysis will be carried on only for the bit synchronization circuit which decides which C/A epoch out of the 20 is coincident with the data bit boundary.

The C/A code is a pseudo random noise chip stream unique in pattern to each satellite and as was mentioned earlier repeats once every millisecond. It is relatively easy for the receiver to match and lock

Figure 1. GPS Message Timing Structure.



CHECK FOR TRANSITION EACH 1/20 DATA BIT, $E_b/N_0 = E_{b0}/N_0 - 13 \text{ dB}$



*X1 EPOCH SETS COUNTER WHEN TRACKING P DATA

Fig. 2. C/A BIT SYNC RESOLUTION & NAV DATA DETECTION

onto the C/A code because the code search is limited to time interval of 1 millisecond and the chip rate is only one tenth of that of the P code. Thus for the analysis to follow we assume that the local C/A code generator is in lock with the incoming code. Consequently, the C/A code epochs are at our disposal.

Figure 1 shows the timing structure of the received GPS signal and Figure 2 shows the C/A bit synchronization resolution circuit. The working of the circuit can be described briefly as follows.

The bit sync circuit operates by checking for data transitions around each epoch (20 possible epochs per bit). There are 20 accumulators keeping track of the transitions scored by a particular epoch. After one of the accumulators fills up to $2^6 = 64$ counts, the associated epoch is declared to be the data bit boundary and the data clock is set accordingly. The data clock is used to provide the timing for the 20 millisecond integrate and dump circuit for the data detector.

In order to simplify hardware, the possible data transition is determined by looking at portions of $1/20$ bit as shown. The transition detector shown in Figure 2 can be a simple comparator. Notice that since only $1/20$ of a bit is integrated, the signal-to-noise ratio degrades by 13 dB. To compensate for this degradation, the accumulators are used. The signal-to-noise ratio improvement is proportional to the number of transitions observed before declaring "lock."

2. Mathematical Modeling

As said above, the transition detector has twenty different output ports, each output is recorded by an accumulator attached to it. We also know that for every bit time there is only one C/A epoch coinciding with the bit boundary. And if a transition in bits is present then that

port will put out a 1 (transition present) with a high probability (we will call this port the correct port) and at the same time all the remaining ports will have zeros with high probability. The procedure will repeat everytime there is a transition in bit putting a '1' in the accumulator attached to the correct port. This continues until the accumulator overflows announcing the boundary of the bit at the C/A epoch associated with the correct port. Assuming uncorrelatedness of the one bit decision and the transition detector decision from the current bit slice under observation to the previous bit slice it is easy to write down the probability of a correct decision. Assuming 'L' is the length (number) of 1's at which the accumulator will overflow ($\log_2 L$ = number of stages of the accumulator)

$$\text{Prob[Correct Decision]} = \sum_{k=L}^{\infty} \{P_1^L (1-P_1)^{k-L} \binom{k-1}{L-1} \left[\sum_{m=0}^{L-1} P_0^m (1-P_0)^{k-m} \binom{k}{m} \right]^{19}\}$$

where P_1 = Probability of detecting a transition at the correct port

P_0 = Probability of detection a transition at any one of the incorrect ports

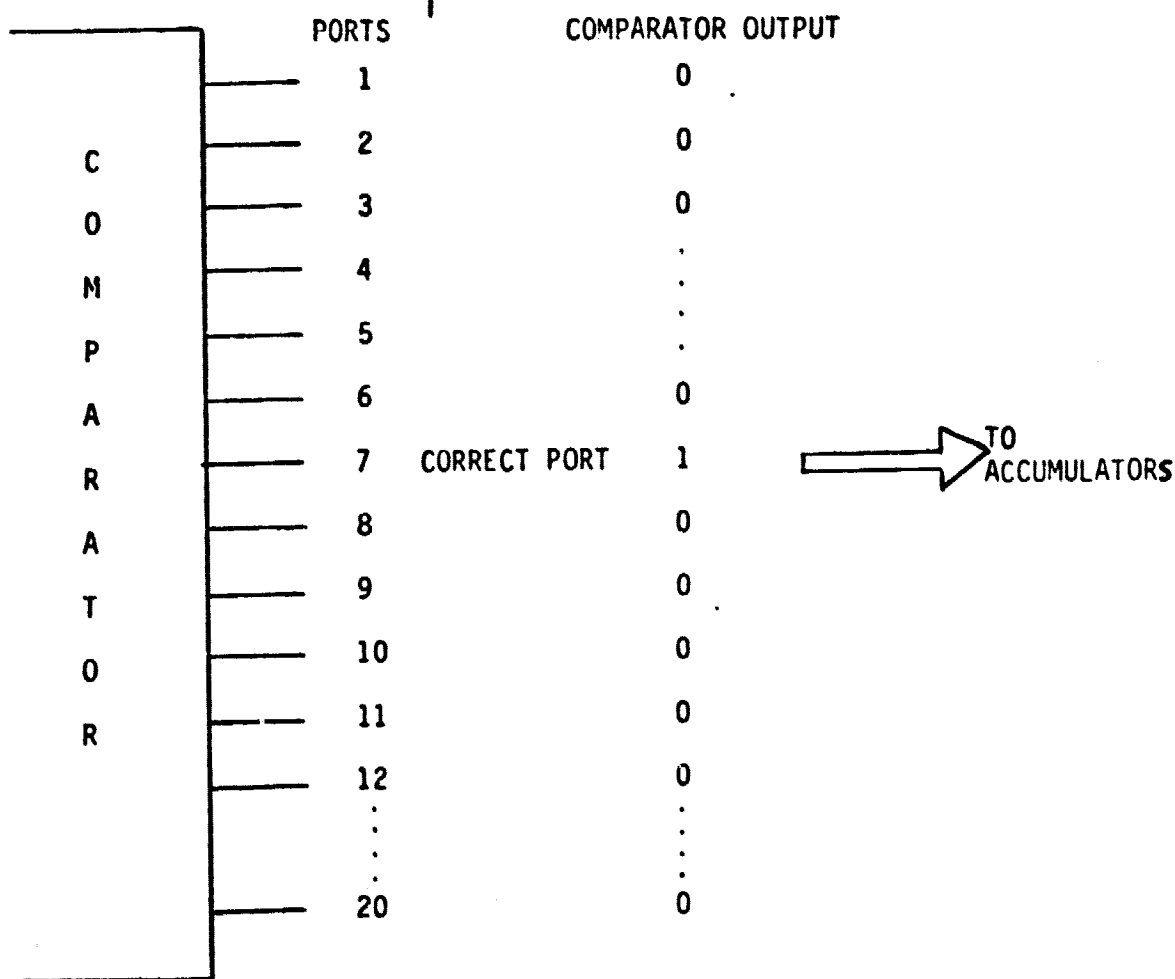
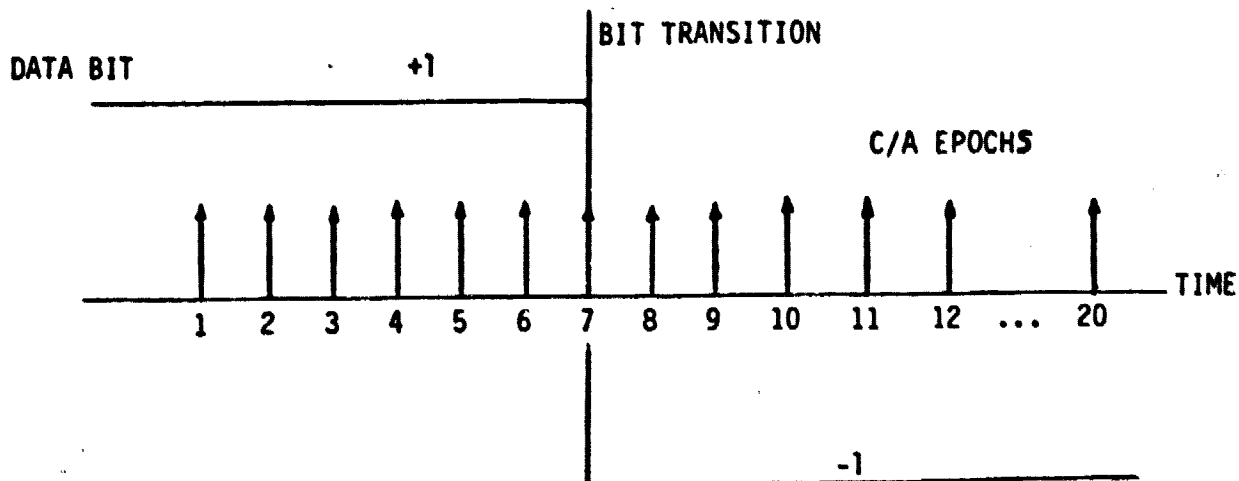
Assuming that transition and nontransition of bits are equally likely, we get

$$P_1 = 0.5$$

where $P_0 = 2P(e)[1-P(e)]$
 $P(e)$ = Probability of deciding ± 1 given ∓ 1 was transmitted

$$= \int_{\sqrt{E_b/N_0}}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\gamma^2/2} d\gamma$$

E_b/N_0 is the bit signal to noise ratio.



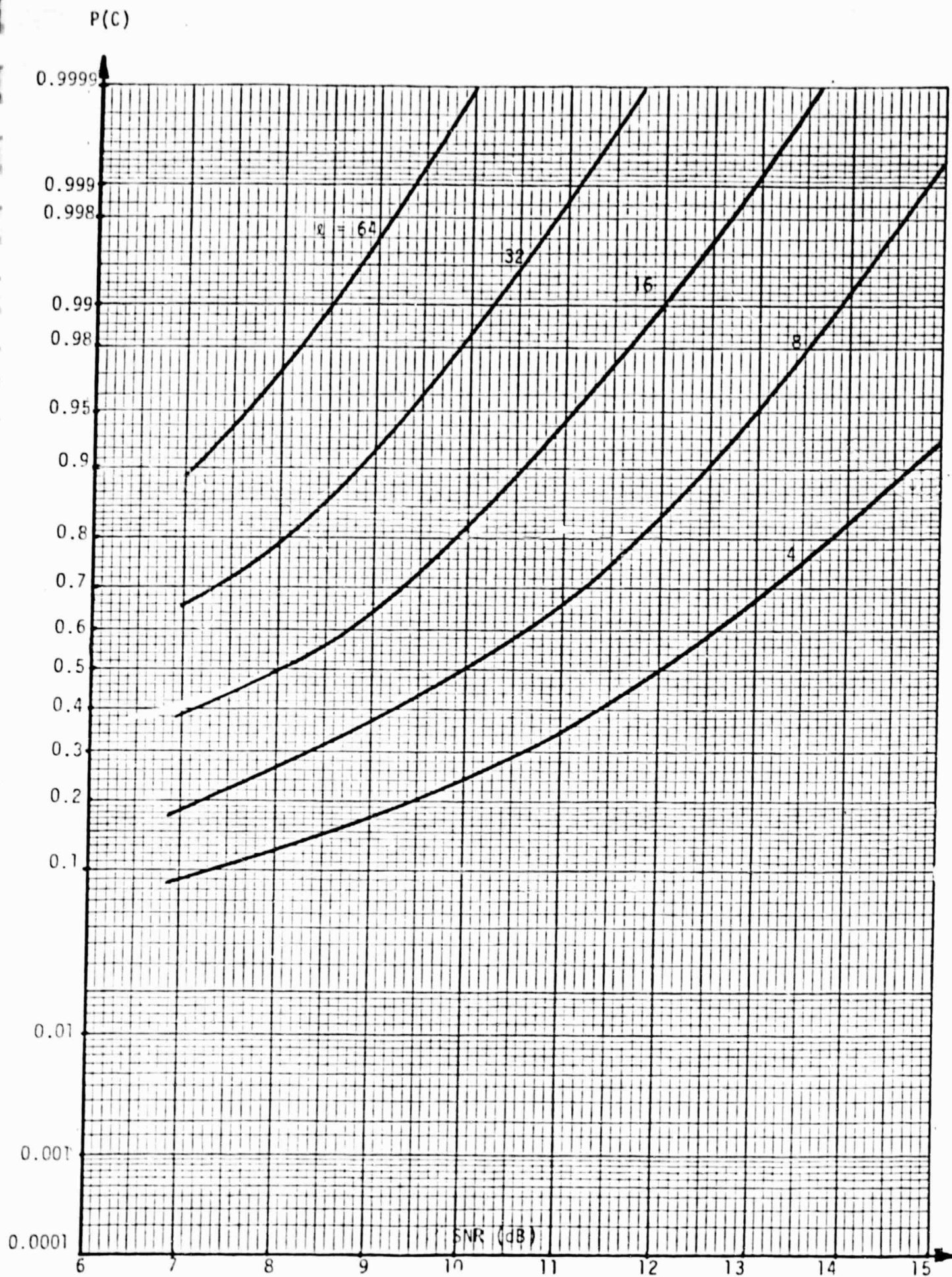


Figure 4. Probability of Correct Detection vs SNR.

Next, we would like to find the average waiting time given that a correct decision is made. This can be written down as

$$\begin{aligned} \text{Average Waiting Time} &= \sum_{k=\ell}^{\infty} k p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} \\ &= \frac{\ell}{p_1} \quad (\text{see Appendix}) \end{aligned}$$

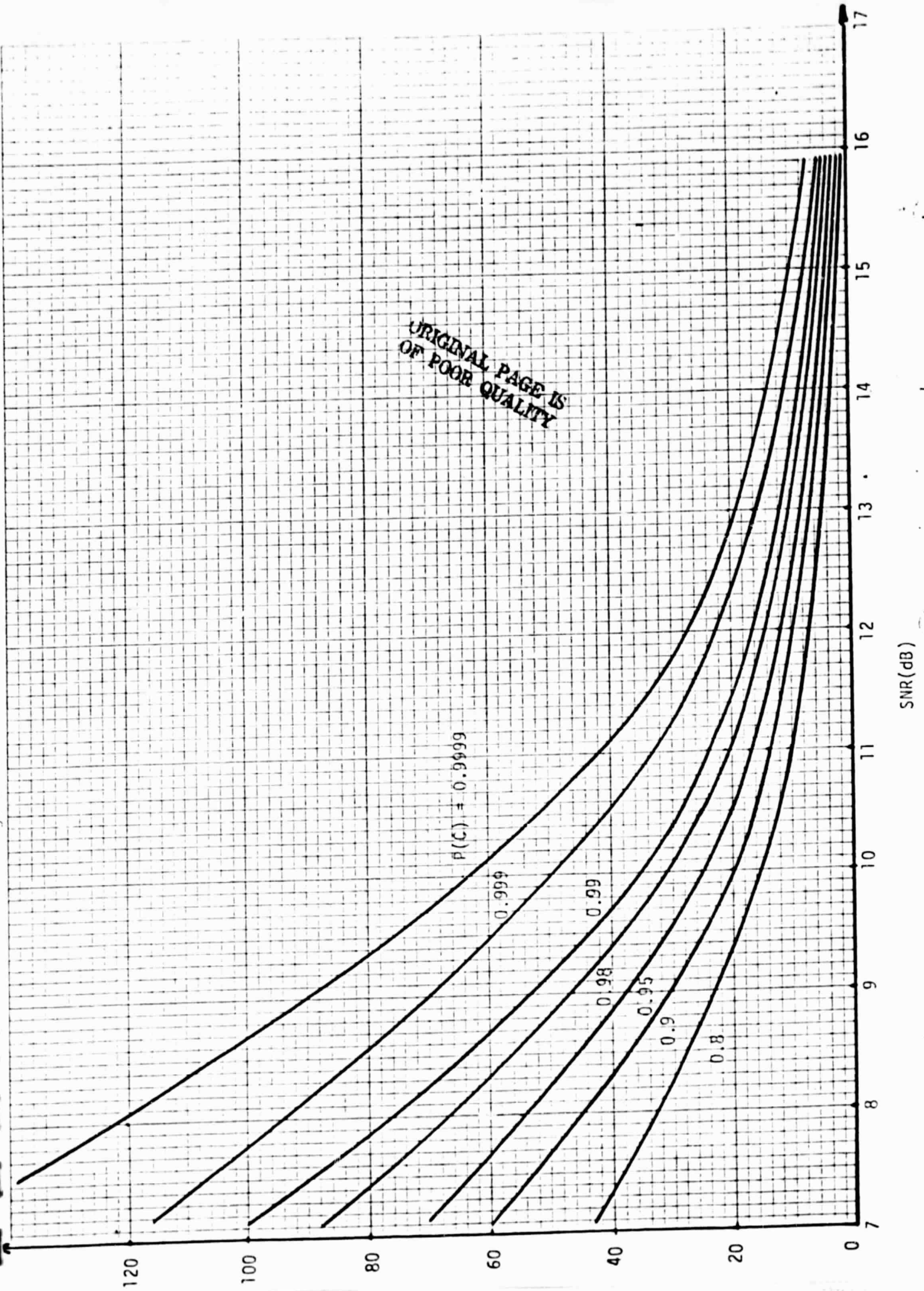
this is a general result, but in our case we have $p_1 = 0.5$; hence, the average waiting time for the shift register length of $\log_2 \ell$ is 2ℓ .

Figure 3 shows the variation of $P(C)$ with respect to threshold ' ℓ ', SNR being the parameter. As can be seen, for low SNR (E_b/N_0) such as 8 dB even the threshold of 64 (i.e. shift register length of 6) gives probability of correct detection to be no more than 0.975. But for high SNR's say 15 dB, even a threshold of 16 gives a probability of correct detection to be in excess of 0.9999. Figure 4 depicts $P(C)$ vs SNR with the threshold ℓ to be the parameter.

Figure 5 plots ' ℓ ' vs the SNR (dB) with $P(e)$ to be the parameter. For example with the SNR of 11 dB and a desirable probability of correct detection of 0.9999 we can see that the threshold requirement is about 42.

It should be pointed out that throughout this analysis the uncorrelatedness of the decision making process for the adjacent bit slices was assumed resulting in uncorrelatedness of the consecutive input of the comparator. Actually there does exist some nonzero correlation between the two consecutive outputs of the correlator which makes our results slightly pessimistic.

Figure 2: Threshold γ_t vs SNR.



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3. Conclusions

For a probability of correct detection of the bit boundary to be 0.99 and a reasonable E_b/N_0 of about 10 dB it will require a shift register length of the accumulators to be 5. This arrangement will require on the average 64 data bits or about 1.2 seconds of time to detect the data bit boundary.

At a low SNR such as 8 dB to obtain the probability of correct detection to be 0.99 will require 7 shift registers in the accumulator and which in term imposes an average waiting time of about 256 data bits or about 5 seconds.

APPENDIX

Let

$$S_{\ell} = \sum_{k=\ell}^{\infty} p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1}$$

It can be shown that

$$S_{\ell} = \sum_{k=\ell}^{\infty} p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} = p_1 \left(\frac{p_1}{1-p_1} \right)^{\ell} \sum_{k=1}^{\infty} (1-p_1)^k \binom{k}{\ell}$$

let $1-p_1 = q_1$

$$S_{\ell} = p_1 \left(\frac{p_1}{q_1} \right)^{\ell} \sum_{k=\ell}^{\infty} q_1^k \binom{k}{\ell}$$

$$\begin{aligned} S_1 &= \frac{p_1^2}{q_1} \sum_{k=1}^{\infty} q_1^k k = \frac{p_1^2}{q_1} \left\{ q_1 \frac{d}{dq_1} \sum_{k=1}^{\infty} q_1^k \right\} = p_1^2 \frac{d}{dq_1} \left\{ \sum_{k=1}^{\infty} q_1^k \right\} \\ &= p_1^2 \frac{d}{dq_1} \left\{ \frac{1}{1-q_1} \right\} = \frac{p_1^2}{(1-q_1)^2} \end{aligned}$$

$$\begin{aligned} S_{\ell+1} &= p_1 \left(\frac{p_1}{q_1} \right)^{\ell+1} \sum_{k=\ell+1}^{\infty} q_1^k \binom{k}{\ell+1} \\ &= p_1 \left(\frac{p_1}{q_1} \right)^{\ell+1} \left[q_1^{\ell+1} + \sum_{k=\ell+2}^{\infty} q_1^k \binom{k}{\ell+1} \right] = p_1 \left(\frac{p_1}{q_1} \right)^{\ell+1} \left\{ \sum_{k=\ell}^{\infty} q_1^{k+1} \binom{k}{\ell} + \sum_{k=\ell+1}^{\infty} q_1^{k+1} \binom{k}{\ell+1} \right\} \\ &= \left(\frac{p_1}{q_1} \right) q S_{\ell} + q_1 S_{\ell+1} \end{aligned}$$

giving us

$$S_{k+1} = \frac{p_1}{1-q_1} S_k$$

Hence

$$S_k = \left(\frac{p_1}{1-q_1}\right)^{k-1} S_1 = \left(\frac{p_1}{1-q_1}\right)^{k-1} \times \frac{p_1^2}{(1-q_1)^2} = \left(\frac{p_1}{1-q_1}\right)^{k+1}$$

Since $q_1 = 1-p_1$ we have

$$S_k = \sum_{k=\ell}^{\infty} p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} = \left(\frac{p_1}{p_1}\right)^{\ell+1} = 1$$

Now we will proceed ahead to find

$$\begin{array}{l} \text{Average} \\ \text{Waiting} \\ \text{Time} \end{array} = \sum_{k=\ell}^{\infty} k p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1}$$

we know that

$$\sum_{k=\ell}^{\infty} p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} = 1$$

$$\therefore \frac{\partial}{\partial p_1} \left[\sum_{k=\ell}^{\infty} p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} \right] = 0$$

$$\sum_{k=\ell}^{\infty} \ell p_1^{\ell-1} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} - \sum_{k=\ell}^{\infty} p_1^{\ell} (k-\ell) (1-p_1)^{k-\ell-1} = 0$$

$$\ell \left(\frac{1}{p} + \frac{1}{1-p} \right) \underbrace{\sum_{k=\ell}^{\infty} p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1}}_{=1} = \frac{1}{(1-p_1)} \sum_{k=\ell}^{\infty} k p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1}$$

Therefore

$$\sum_{k=\ell}^{\infty} k p_1^{\ell} (1-p_1)^{k-\ell} \binom{k-1}{\ell-1} = (1-p_1) \left(\frac{1-p+p}{(1-p)p} \right)^{\ell} = \frac{\ell}{p_1}$$

REFERENCE

- [1] C. M. Chie, "Bit Synchronization and Message Demodulation for GPS Signal, LinCom Memo GPS-81-CMC-2, February 1981.